A 1.8V Gb/s LVDS Transceiver in 0.35μm CMOS

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Abstract

A CMOS transceiver circuit operating at 1Gb/s for application of low voltage differential signal (LVDS) standard is presented. The circuit operates functionally at a wide range of power supply voltage from 1.8 to 3.6V. A test chip is designed and implemented by using TSMC 3.3V 0.35μm 1P4M CMOS process, and its core size is 240μm*263μm.

Keywords

LVDS, transmitter, receiver, transceiver

1. Introduction

LVDS (low voltage differential signal) is a data transmission standard for data rate up to 500Mb/s [1]. Low voltage swing can minimize the power dissipation and enable operation at very high speed. Differential signal with opposite current/voltage swing is to enhance noise immunity. It is designated for high speed data transmission. An even higher data rate is required for future applications.

The LVDS interface, as shown in Fig. 1, can be simply modeled as a transmitter, a receiver and interconnection between them. A simplified circuit model of transmitter is shown in Fig. 2. The interconnection and receiver are regarded as a 100Ω terminating resistor. When transistors M1 and M3 are turned ON by the *Data* signal, M2 and M4 will be turned OFF by *Data'*. The current is flowing into the interconnection as shown in Fig. 2. A voltage V_{od} will then be generated across the terminating resistor with a magnitude of I*100(V). Oppositely, when transistors M2 and M4 are turned ON, M1 and M3 will be turned OFF. The current flows in opposite direction through the interconnection. A negative voltage will then be generated across the resistor.

The circuit model of receiver is shown in Fig. 3. The receiver is modeled as a comparator with a 100Ω terminating resistor. The receiver can generate output of '1' or '0' by detecting the polarity of input differential voltage V_{od} ($V_{ia} - V_{ib}$). If the polarity of V_{od} is positive, the output of receiver will be '1'. If the polarity of V_{od} is negative, the output of receiver will be '0'. The terminating resistor at the receiver provides current-to-voltage conversion as well as impedance matching.

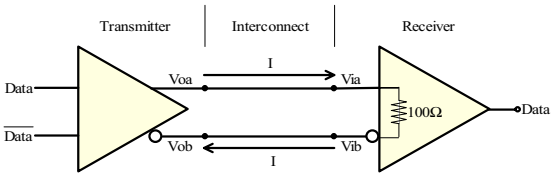

Figure 1. LVDS Interface

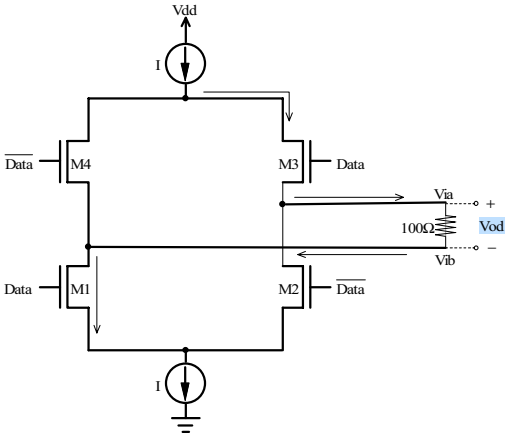

Figure 2. A Simplified Model of Transmitter

2. Circuit Design

2.1 Transmitter

Based on the circuit model in Fig. 2, a transmitter is implemented as shown in Fig. 4. M1-M4 are acting as current switches which control the flowing direction of current in the terminating resistor. Mp and Mn serve as current source and current sink respectively. The differential signal of the transmitter must confirm the specifications of LVDS standard:

$$250mV \le |V_{od}| \le 400mV \quad (1);$$

$$1125mV \le V_{os} \le 1275mV \quad (2).$$

where V_{od} is the differential output voltage, and V_{os} is the common-mode voltage of the differential output voltage.

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In order to keep the circuit operating in a wide range of power supply from 1.8 to 3.6 V, an additional difference amplifier is included to provide a fixed bias for Mp regardless of V_{dd}'s variation. The voltage 1.2V, which is derived from a bandgap voltage reference circuit [3], tied to node A anchors the V_{os} at 1.2V and the difference amplifier can generate a voltage of Vdd-1.2V to provide a fixed Vgs (1.2V) for Mp. Hence, the current flowing through Mp can be derived from the following formula,

$$I(Mp) = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \qquad (3)$$

Since the V_{gs} of Mp is fixed, we can design the current of Mp by adjusting the W/L ratio of Mp. If the ratio of Mp is also fixed, the current of Mp is fixed too. That's, we can fix the V_{od} at 400mV by designing a 4mA current flowing into the terminating resistor.

The difference amplifier is implemented as shown in Fig. 5. When the resistor ratio $R_1/R_2 = R_3/R_4$, its output V_o will be $R_2/R_1*(V_2-V_1)$. The value of V1 and V2, as shown in Fig. 4, are 1.2V and V_{dd} respectively. When the output of the difference amplifier is connected to the gate of Mp, then the Vgs of Mp will be fixed at 1.2V. Similarly, we connect the 1.2V to the gate of Mn, then the Vgs of Mn is also fixed at 1.2V. To minimize the chip size, these four resistors are realized by using four identical transistors operating at a same bias.

A two-stage amplifier [3], implemented as shown in Fig. 6, is used for the operational amplifier of difference amplifier. The first stage (M1-M4) is a differential amplifier that provides gain for the differential input. The second stage (M5) is a source follower which has the capability to drive output and has a better frequency response. By adequate design, the circuit needs not any compensation capacitance and thus saves the chip size. M6 and M7 are current mirror to provide bias currents. M8 and M9 form a voltage divider to provide gate voltage for M6 and M7. Since the drain of M9 is tied to 1.2V, the gate voltage of M6 and M7 is independent of V_{dd}, consequently the bias current of the circuit is also independent of V_{dd}.

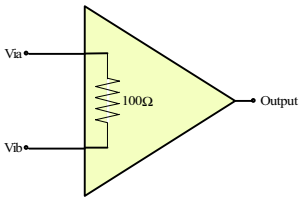

Figure 3. Circuit Model of Receiver

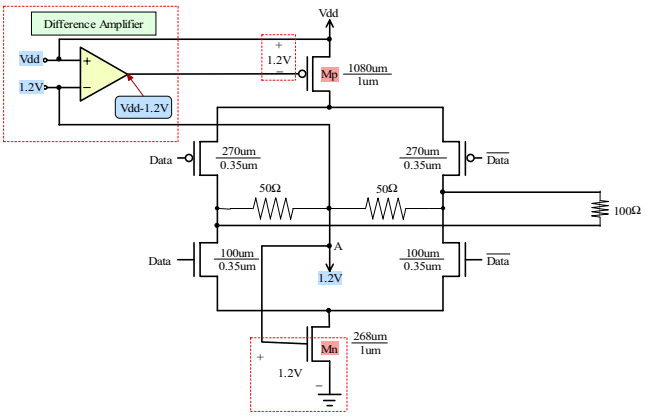

Figure 4. Circuit of Transmitter

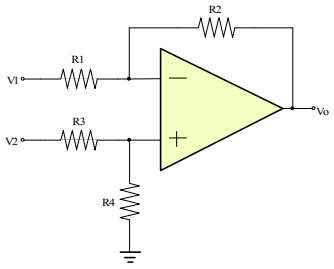

Figure 5. Circuit of Difference Amplifier

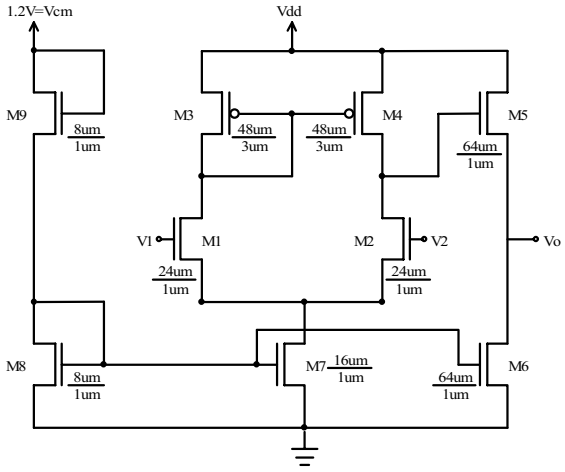

Figure 6. Circuit of Operation Amplifier

2.2 Receiver

The designed receiver is shown in Fig. 7. The receiver consists of 100Ω terminating resistor, five differential amplifiers (DAmp) and one complementary self-biased differential amplifier (CSDA) [2]. The differential amplifier uses diode-connected transistors as active load, as shown in Fig. 8. The advantages of the differential amplifier are simple and it has two symmetrical outputs. Although the gain of the differential amplifier is poor, yet it can be easily cascaded to achieve a high gain. We would get a high gain at high speed by cascaded 5 stages.

The circuit of complementary self-biased differential amplifier is shown in Fig. 9. The circuit can provide large switching currents and it is suitable for high-speed comparator. Moreover, it can convert the differential input to single end output.

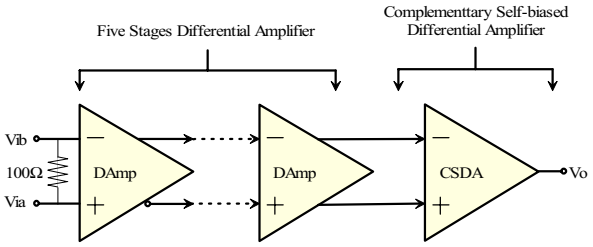

Figure 7. Circuit diagram of receiver.

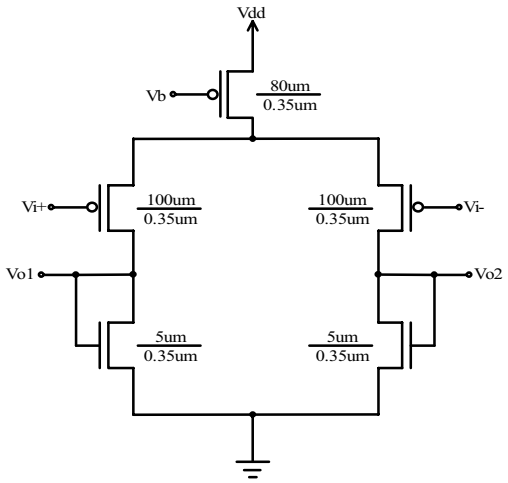

Figure 8. Circuit diagram of DAmp.

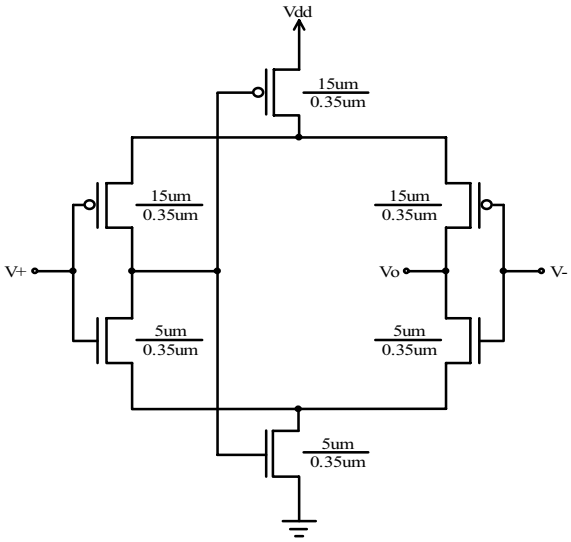

Figure 9. Circuit Diagram of CSDA

3. Simulation and Implementation

The simulation of difference amplifier is shown in Fig. 10. We can see that the output of difference amplifier is equal to V_{dd}-1.2V. According to the simulation result, when V_{dd} is reduced from 3.6V to 2.2V, the differential signal V_{od} of the transmitter will be reduced from 400mA to 350mA due to channel length modulation. The simulation result of transmitter which operates at V_{dd}=1.8V is shown in Fig. 11. The four waveforms in Fig. 11, from top to bottom, are input, two outputs and the differential signal V_{od} of the transmitter. When V_{dd} is 1.8V, V_{od} decreases to about 300mV, because the current source of transmitter can not operate in saturation region appropriately at such low operating voltage. Nevertheless, 300mV still fits the LVDS standard. The simulation of a loop test on the whole circuit is shown in Fig. 12. The five waveforms in Fig. 12, from top to bottom, are the input to transmitter, the two outputs of transmitter (loop back to the two inputs of receiver), V_{od} of transmitter and the output of the receiver. The specifications of our designed transceiver comparing with the LVDS specifications are listed in table 1.

The chip was designed and fabricated by using TSMC 0.35μm 1P4M CMOS process. The layout of the transceiver is shown in Fig. 14. Its core size is 240μm*263μm (448μm*481μm if I/O pads included). According to the simulation results, the circuit can operate at 1Gb/s, the power consumption of transmitter is 12mW at supply voltage of 1.8V and receiver is 19mW at supply voltage of 3V. The measurement result for a loop test is shown in Fig. 13. Due to the limitation of our instrument, the measurement was only done at a lower frequency. A higher frequency testing will be reported at the conference.

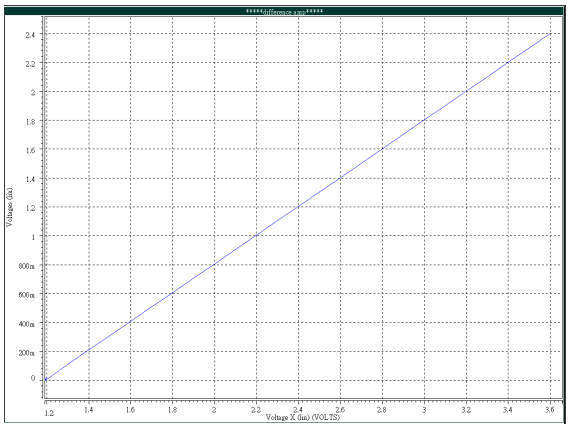

Figure 10. Simulation of Difference Amplifier

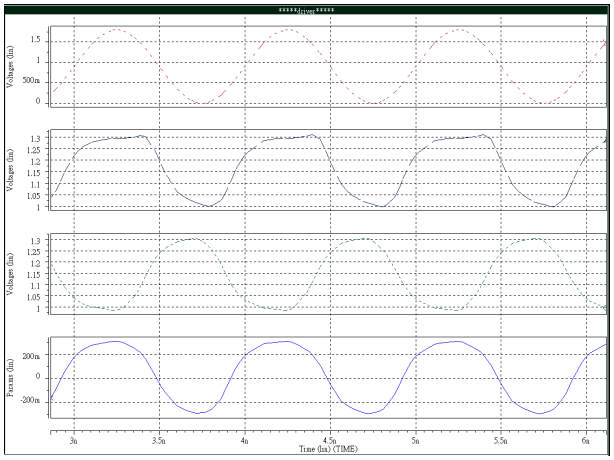

Figure 11. Simulation of Transmitter (V_{dd}=1.8V, f=1GHz)

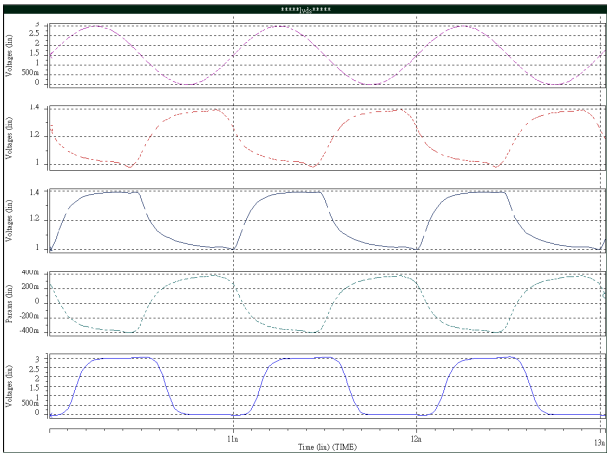

Figure 12. Simulation of Loop Test (V_{dd}=3V, f=1GHz).

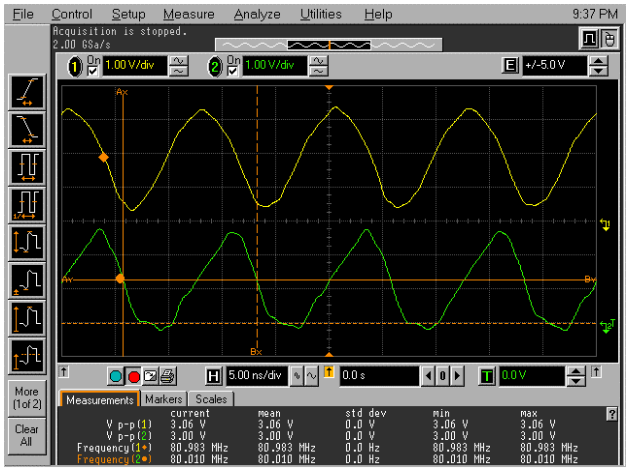

Figure 13. Measurement of Loop Test.

4. Conclusion

In this paper, the design and implementation of transmitter and receiver circuits for low voltage differential signal (LVDS) standard operating at 1Gb/s are presented. The transmitter is designed for operating at a wide range of power supply voltage from 1.8V to 3.6V by using a difference amplifier to provide a fixed bias independent of power supply. The chip is fabricated by using TSMC 3.3V 0.35µm 1P4M CMOS process, and its core size is 240µm*263µm. The power consumption of transmitter is 12mW at supply voltage of 1.8V and receiver is 19mW at supply voltage of 3V.

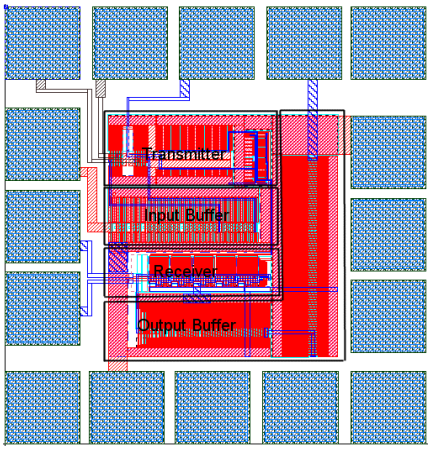

Figure 14. Layout of the chip

Table 1. Summary of Specifications

Transmitter	Ours		LVDS	
	Min	Max	Min	Max
Voh		1400mV		1475mV
Vol	1000mV		925mV	
Vod	300mV	400mV	250mV	400mV
Vos	1150mV	1250mV	1125mV	1275mV
Receiver	**Ours**		**LVDS**	
	Min	Max	Min	Max
Vidth	-100mV	100mV	-100mV	100mV
Rin	90Ω	110Ω	90Ω	110Ω

References

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