A Fault Model for Cross-Check Test on Infrared FPA

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Abstract:

The increase of array size and decrease of cell size make the testing of infrared focal plane array (FPA) being very difficult. A design for test scheme, cross-check test, for infrared focal plane array (FPA) is presented in this paper. For an array size of M by N, the testing times can be reduced from the order of M*N to M+N. A fault model for cross-check test on FPA is also proposed and analyzed in this paper.

Keywords: FPA, Cross-Check Test, Readout, Design for Test, Fault Model

I. Introduction

Recently, large array format and small pixel size are indispensable to achieve high-resolution infrared (IR) focal plane array (FPA) applications for uses in military, medical and astronomy [1-6]. In general, an IR FPA consists of two major parts : a sensor array and a readout circuit [1,8,9]. The sensor array may be constructed by a two dimensional array of photovoltaic detectors. In Fig. 1, an InSb P-N junction device [1,3,5] is one type of photovoltaic detector. Its I-V characteristic curve when exposed to IR radiation is shown in Fig 1(b). The readout circuit is designed to condition the detector and provide an interface to pick up the detector signal for subsequent signal processing stage. For the issues of cost and compatibility, the readout circuit is now commonly using CMOS technology [8-11]. The readout circuit chip and the sensor array chip are compounded face to face by flip chip technology [6-7], as shown in Fig. 2, where indium bumps are grown on the aligned pixels of both chips.

The increase of array size and decrease of cell size of FPA will unavoidably impose on the possibility of defect occurrence during manufacturing and flip chip process. Hence, it is urgent to include a design for test scheme to economically test the detector array and readout chips of a large array size FPA. To test the readout circuit, current sources built in the readout circuit itself to replace the function of sensor cell during testing had been proposed [12-16]. To test the sensor array before the flip chip process, the sensor cell can be probed directly for measuring its I/V characteristic [18]. Nevertheless, the total probe time will be proportional to the array size and become unacceptable when the array size grows large. Beside that, the probe contact for small cell size will have the uncertainty problems. In [19], a modification on the cell selection in FPA had been proposed to calibrate the dark current by a series of measurements at different selection modes. All the above methods test a cell each time, for an array size of M by N, at least M*N times of testing are required to test all cells once. To reduce the total number of testing times, a parallel test scheme, called cross-check test, was proposed by the authors in [20]. Column by column and row by row, parallel test is performed with a modified cell selection maneuver. Hence, the testing times can be reduced from the order of M*N to M+N. In this paper, the cross-check test scheme for FPA is reexamined in section II. Based on the test scheme, a fault model and its detectability are unveiled in section III. Finally, a conclusion is made in the last section.

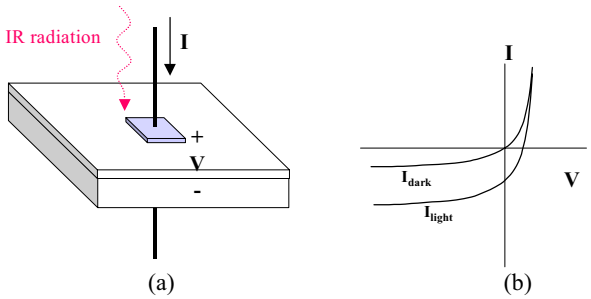

Fig. 1: An IR photovoltaic detector

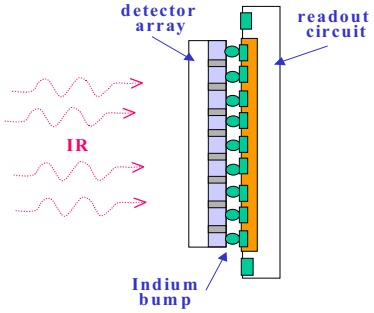

Fig. 2: A flip-chip binding

II. The Cross-Check Test Scheme

A readout circuit for FPA is shown in Fig. 3. It consists of a row decoder, a column selector, and a two-dimensional array of unit cells for sensor readout. The unit cell, as demonstrated in Fig. 4, contains a bump pad for sensor binding, a readout circuit, and a row-select MOS switch. Each sensor cell in the FPA will be sequentially accessed through the operations on row and column selection lines. The row decoder and the column select are generally realized by a shift register, as shown in Fig. 5,

with MOS selecting switches. The shift register is basically a cyclic one with *load*, *clear* and *preset* functions. In normal operation, only one DFF in row shift register and one DFF in column shift register are set to activate the row and column MOS switches respectively. Hence, a row is addressed and a cell in the addressed row is selected, as shown in Fig. 6. The other cells in the addressed row are sequentially selected, then follow through the cells of the other rows.

Before the flip chip binding, the bump pad is floating, hence the readout circuit can not operate functionally and be tested. A possible testing method is to include a current source, as shown in Fig. 4, attached to the bump pad. The function of photo-sensor will be replaced, during testing, by the built-in current source that can provide a current to the readout circuit.

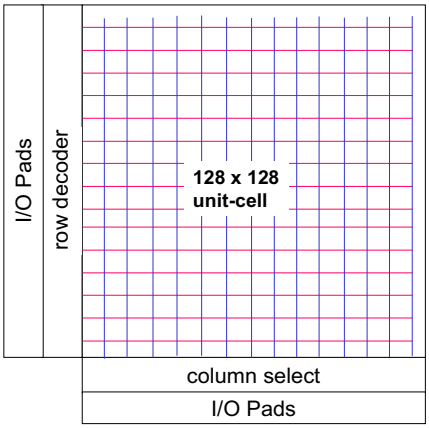

Fig. 3: The architecture of the readout circuit

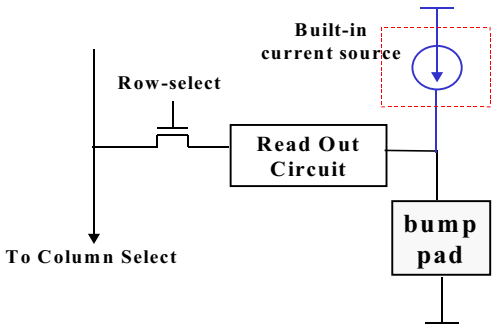

Fig. 4: The unit cell of readout circuit

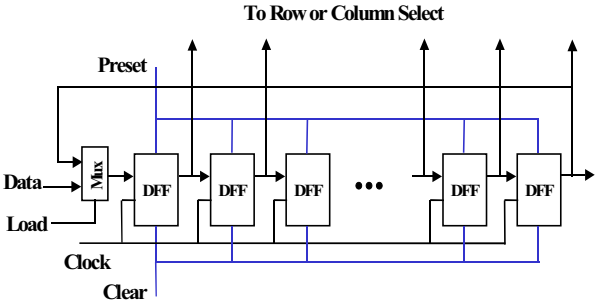

Fig. 5: The shift register

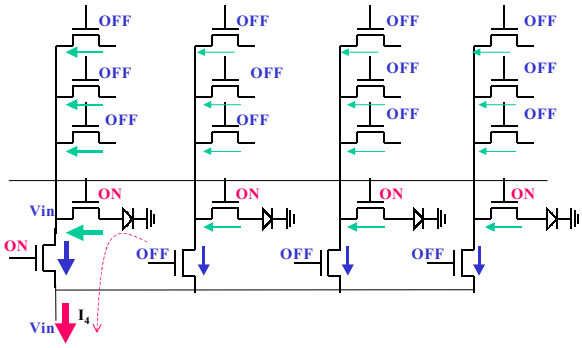

Fig. 6: The selection of a detector

To test a FPA of large array size, conventional methods need at least M*N times of test to exercise all cells (for convenient, we assume that M is the number of columns and N is the number of rows). When the array size grows large, the testing time becomes unacceptable. In order to reduce the test times, resemble the idea proposed in [19], a parallel test scheme, called cross-check test, is proposed in [20] by the authors. The test times can be thus reduced from the order of M*N to M+N.

To perform cross-check test, the shift register in readout circuit must have the functions of *clear*/*preset* and *load*. The shift register shown in Fig. 5 can perform these functions. With these functions, the pattern in the shift register can be controlled. In normal operation, each time, only one row and one column are activated, that is, only one DFF in the shift register is ON. To perform a parallel test, it demands that all rows and all columns could be intentionally selected ON. Hence, we can select all rows or all columns for parallel test. That is, for example, if a full row of cells are needed to be tested in parallel, the DFF for the tested row in row shift register should be ON, and all the DFFs in column shift register should be ON, as shown in Fig. 7. It is similar to parallel test a full column, as shown in Fig. 8.

The cross-check test scheme is to test a full row of cells in parallel for each row, and followed by a full column of cells in parallel for each column. Consequently, row by row and column by column, the number of test times is reduced to M+N. The steps for cross-check test are as follows:

(1) For each row, measure the total currents of one full row. As shown in Fig. 7, all columns are selected ON, and only the interested row is selected ON. Sensors in the interested row will contribute their currents to the measurement. Therefore, if there is no faulty sensor cell in the row, the measured current will be M times of one cell's. And if there are faulty cells, the measured current will be different from the expected value.

(2) For each column, measure the total currents of one full column. As shown in Fig. 8, all rows are selected ON, and only the interested column is selected ON. Sensors in the interested column will contribute their currents to the measurement. Therefore, if there is no faulty sensor cell in the column, the measured current will be N times of one cell's. And if there are faulty cells, the

measured current will possibly be different from the expected value.

From the measurement results of the above two steps, we can cross check them to identify which cell is faulty. For example, if cell (i, j) is faulty, then the measurements of i'th column and j'th row will reflect this fault.

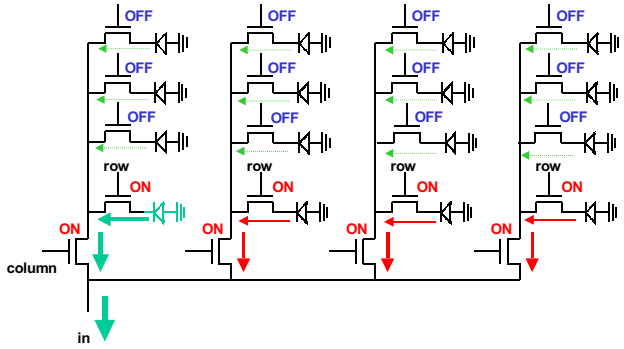

Fig. 7: The selection of one full row

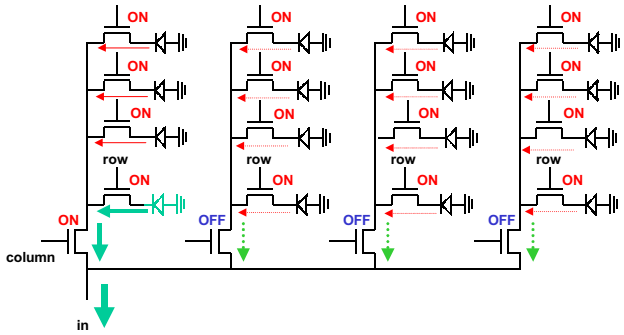

Fig. 8: The selection of one full column

With the built-in current source, as shown in Fig. 4, the readout circuit can be tested before the binding of readout and sensor array chips. After binding, the cells in sensor array can be tested by measuring their dark currents. If the cells are tested one by one, the total testing time will grow into unacceptable when the array size become large. Hence it is desirable to employ parallel test scheme. Cross-check test can perform parallel test, however, there does exist possibility of fault masking. In the next section, we will categorize the possible faults and figure in the fault detectability of cross-check test.

III. Fault Detection of Cross-Check Test

Since the testing is mainly relying on the measurement of current, it is convenient to classify the possible faults, after binding of readout and sensor array chips, into three categories : open fault, short fault and large-current fault, as illustrated in Fig. 9. The open fault, as shown in Fig. 9(a), is caused by an unhealthy binding where the bumps between readout and sensor array chips are not connected. Therefore the bump pad of the readout is floating and no current appears. The short fault, as shown in Fig. 9(b), is also caused by an unhealthy binding where the adjacent bumps are shorting together. Consequently the shorted cells will receive extra currents from each other. The large-current fault, as shown in Fig. 9(c), is caused by bad sensor cell that has a large leakage current. The short fault can be regarded as a type of large-current fault. For simplicity, we will only treat the open fault and large-current fault in subsequent analysis. If the cells in FPA are tested by individually measuring their currents, the open fault and large-current fault can be obviously detected and located. Yet if they are tested by cross-check test in parallel, there does exist possibility of fault masking.

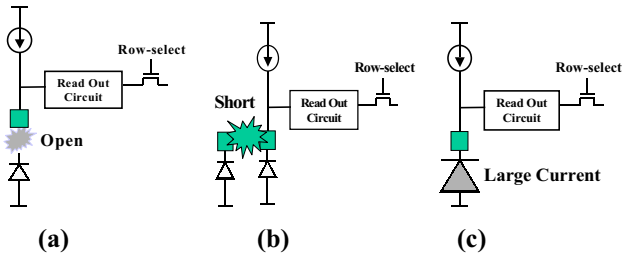

Fig. 9 : (a) open fault, (b) short fault, (c) large-current fault

When only single fault is considered, there does no fault masking exist. All single fault can be evidently detected and located by cross-check test. When double-fault is considered, if only one fault type is allowed, say open fault or large-current fault, then both faults of double-fault can be detected and located. However, if both open and large-current fault types are allowed, then both faults can be detected yet not located in some special cases. For example, as shown in Fig. 10, an open fault and a large-current fault whose current is doubled exist in a same row. In this case, when performing cross-check test, testing row by row can not identify the faulty row due to current cancellation of the two faults. Nevertheless, testing column by column can identify the faulty columns where the two faults belong to. It is similar that when double-fault exists in a same column. If the two faults of double-fault are not exist in the same row or same column, both faults can be detected and located by cross-check test. When higher level of multiple-fault is considered, the possibility of fault masking will increase. And if the faulty cells canceling each other currents by row and column in the same time, then there will be no fault detected, as shown in Fig. 11 for a quadruple-fault case.

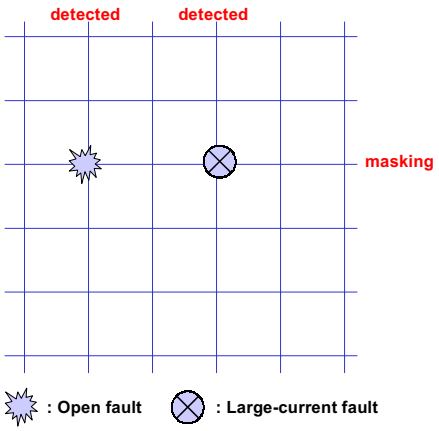

Fig. 10 : A double-fault example

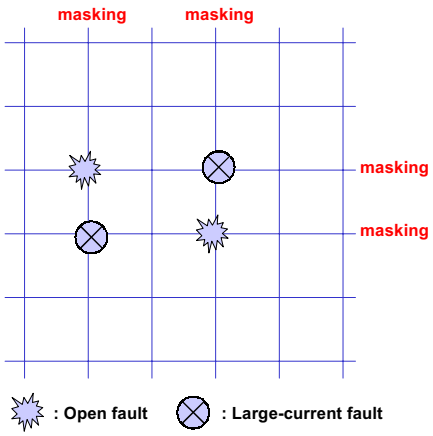

Fig. 11 : A quadruple-faule example

IV. Conclusion

To reduce the test time of FPA in large array size, a parallel test scheme, called cross-check test, is presented in this paper. A full row (or column) of cells can be tested in parallel at the same time. By cross checking the test results of rows and columns, a faulty cell can be easily identified. Applying the proposed cross-check test scheme, the testing time can be speeded up from the order of M*N to M+N. The fault detectability of cross-check test is analyzed based on proposed fault model for FPA. Single fault can be fully detected and located. Double-fault can be detected yet not located in some special cases. Higher level of multiple-fault can result a high possibility of fault masking hence reduce the detectability of cross-check test.

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