A Cross-Check Test Scheme for Infrared Focal Plane Array

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Abstract:

A cross-check test scheme for infrared focal plane array (FPA) is proposed and presented in this paper. A FPA readout circuit chip is proposed to perform this scheme. The testing time for a M by N array can be speeded up via the scheme in a parallel way from the order of M*N to M+N. A built-in test scheme is also employed in the readout circuit for verifying the scheme and testing readout circuit itself.

Keywords:

FPA, Testing, Cross Check, Readout, Built-In Test

I. Introduction

Recently, high-resolution infrared (IR) focal plane arrays (FPA) have been developed for various applications for uses in military, medical and astronomy. A large array format and small pixel size are indispensable to achieve such high-resolution [1-6] for future applications.

In general, an IR FPA is composed of two major parts, a detector array and a readout circuit [1,8,9]. A photovoltaic detector based on an InSb P-N junction device [1,3,5], as shown in Fig 1(a), is used to construct the detector array. The I-V characteristic curve of the detector when exposed to IR radiation is shown in Fig 1(b). Its characteristic is similar to a photodiode. The readout circuit is designed to bias the detector and provide an interface for subsequent signal processing stage. For the issues of cost and compatibility, CMOS technology is now commonly used for the readout circuit implementation [8-13]. A flip chip technology [6-7], as shown in Fig 2, is used to compound the IR detector array and CMOS readout chip by indium bumps which are grown on the aligned pixels of both chips.

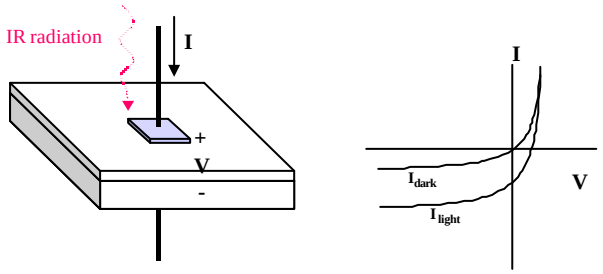

Fig. 1: A photovoltaic IR detector

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Although there are a lots of proposed readout circuit techniques to cancel noise and dark current effects [21-24]. However, the increase of array size and decrease of cell size will unavoidably impose on the possibility of defect occurrence during manufacturing process. Hence, it is necessary to have a quality testing on the detector array and readout chips.

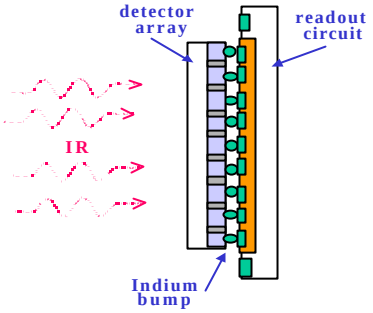

Fig. 2: A flip-chip binding

To test the readout circuit, current sources built in the readout circuit itself to replace the function of sensor cell during testing is proposed [14-18]. To test the sensor array before the flip chip process, the sensor cell can be probed directly for measuring its I/V characteristics [20]. The total probe time will be proportional to the array size and become unacceptable when the array size grows. Beside that, the uncertainty of each probe contact for small cell size will have the problems of accuracy and credibility. In [25], a modification on the selection of cells in FPA had been proposed to calibrate the dark current by a series of measurements at different selection modes. All the above methods test a cell each time, for an array of size M by N, M*N times of testing are required to test all cells once. To reduce the total number of testing times, a parallel test scheme, called cross-check test, is proposed and presented in this paper. Column by column and row by row, parallel test is performed with a modified cell selection maneuver. Hence, the testing times can be reduced from the order of M*N to M+N.

The built-in current source for FPA readout circuit is described in section II. The proposed parallel cross-check test scheme and the test procedure for this scheme are unveiled in section III. A chip for verifying the scheme is demonstrated in section IV. Finally, a conclusion is made in the last section.

II. Built-In Current Source for Readout Circuit

A readout circuit for FPA is shown in Fig. 3. It consists of a row decoder, a column selector, and a two-dimensional array of unit cells for sensor readout. The unit cell, as depicted in Fig. 4, contains a bump pad for sensor binding, a readout circuit, and a row-select MOS switch. Each sensor cell in the FPA will be sequentially accessed through the row and column selection lines. The row decoder and the column select are generally realized by a shift register, as shown in Fig. 5, with MOS selecting switches. The shift register is basically a cyclic one with load, clear and preset functions. In normal operation, only one DFF in row shift register and one DFF in column shift register are set to activate the row and column MOS switches respectively. Hence, a row is addressed and a cell in the addressed row are selected. The other cells in the addressed row are sequentially selected, as shown in Fig. 6. Then follow through the cells of the other rows.

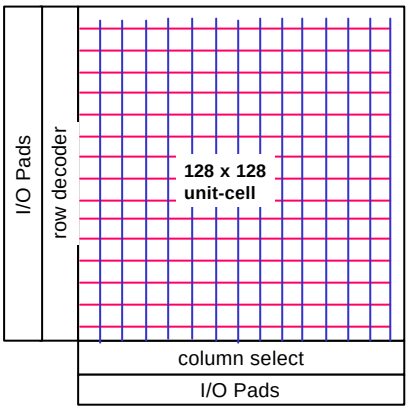

Fig. 3: The architecture of the readout circuit

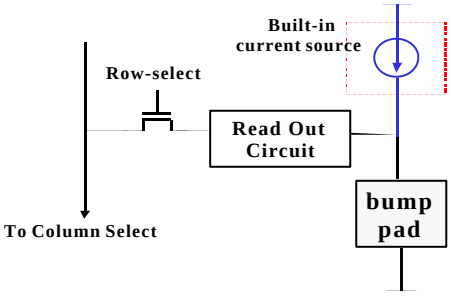

Fig. 4: The unit cell of readout circuit

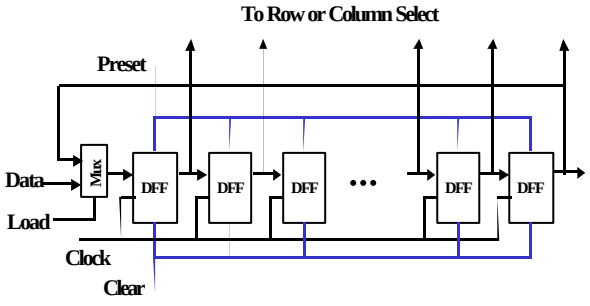

Fig. 5: The shift register

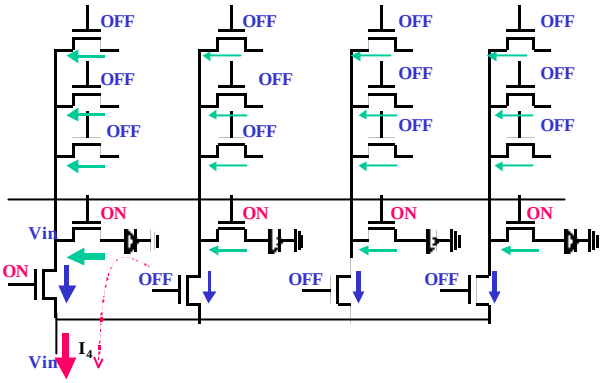

Fig. 6: The selection of a detector

Before the flip chip binding, the bump pad is floating, hence the readout circuit can not operate functionally and be tested. A possible testing method is to include a current source, as shown in Fig. 4, attached to the bump pad. The function of photo-sensor will be replaced by the built-in current source that can provide a current to the readout circuit. This built-in current source can not only test the readout circuit itself before flip chip binding but also can be used to test the yield of binding by open/short test [19].

III. The Cross-Check Test Scheme for FPA

To test a FPA of large array size, conventional methods need at least M*N times of test to exercise all cells (for convenient, we assume that M is the number of columns and N is the number of rows). When the array size grows large, it becomes unacceptable. In order to reduce the test times, resemble the idea in [25], a parallel test scheme, called cross-check test, is proposed. The test times can be thus reduced from the order of M*N to M+N.

To perform cross-check test, the shift register in readout circuit must have the functions of clear/preset and load. With these functions, the pattern in the shift register can be controlled. In normal operation, each time, only one row and one column are activated, that is, only one DFF in the shift register can be ON. To perform a parallel test, it demands that all rows and all columns can be intentionally selected ON. Hence, we can select all rows or all columns for parallel test.

The cross-check test is to test a full row of cells in parallel for each row, and followed by a full column of cells in parallel for each column. Consequently the number of test times is reduced to M+N. The steps for cross-check test are as follows:

(1) For each row, measure the total currents of one full row. As shown in Fig. 7, all columns are selected ON, and only the interested row is selected ON. Sensors in the interested row will contribute their currents to the measurement. Therefore, if there is no faulty

sensor cell in the row, the measured current will be M times of one cell's. And if there are faulty cells, the measured current will be different from the expected value.

(2) For each column, measure the total currents of one full column. As shown in Fig. 8, all rows are selected ON, and only the interested column is selected ON. Sensors in the interested column will contribute their currents to the measurement. Therefore, if there is no faulty sensor cell in the column, the measured current will be N times of one cell's. And if there are faulty cells, the measured current will possibly be different from the expected value.

From the measurements of the above two steps, we can cross check them to identify which cell is faulty. For example, if cell (i, j) is faulty, then the measurements of ith column and jth row will reflect this fault.

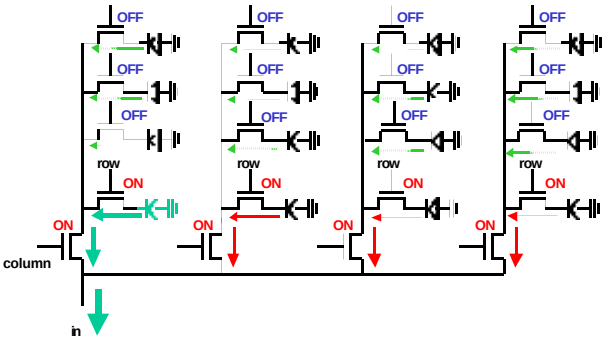

Fig. 7: The selection of one full row

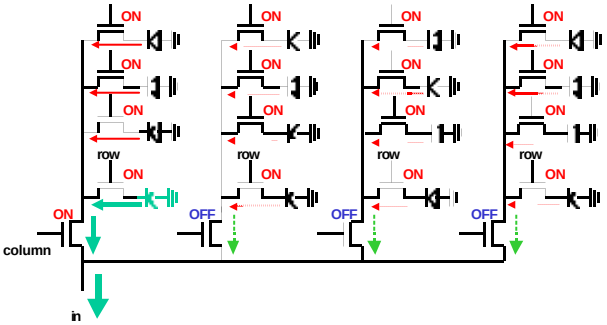

Fig. 8: The selection of one full column

IV. Verification

To verify the proposed cross-check test scheme, we had designed a 4*4 FPA readout circuit. The photograph of the readout circuit is shown in Fig. 9. It had been fabricated by using UMC 0.5um 2P2M CMOS process provided by MPC service of Chip Implementation Center (CIC).

Without the flip chip binding of IR sensor chip, we use the built-in current source to generate current for testing each readout cell. First, we test the chip in normal operation and measure the current of each cell. Then we apply the cross-check test to verify the correctness of the scheme for fault-free case. After that, we use laser cutter to damage the built-in current source of a cell, and apply the cross check test to identify the damaged cell. The results are just what we expected.

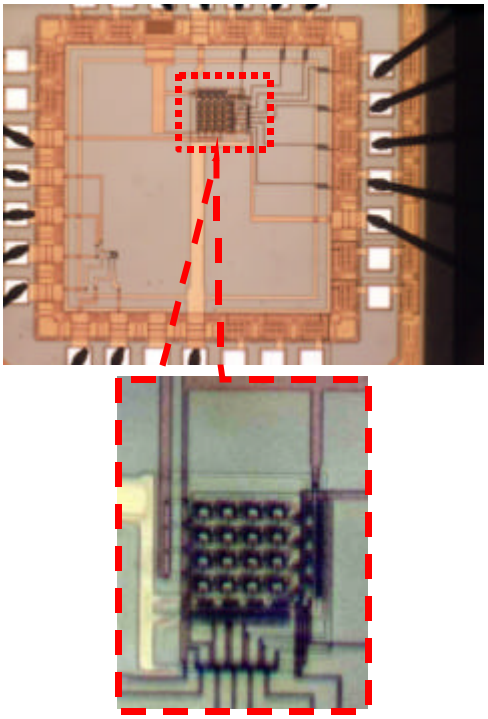

Fig. 9: The photograph of a 4*4 FPA readout circuit

The proposed cross-check test scheme were proven to work out well if there is only one faulty cell at a time. However, in realistic case, there may exist multiple faulty cells in the same time. And these multiple faulty cells may have faulty effect to cancel each other, which will make the cross-check test ineffective. Hence, it needs more discussion on the testability of cross-check test scheme when multiple faulty cells are considered.

V. Conclusion

To reduce the test time of FPA in a large array size, a parallel test scheme, called cross-check test, is proposed and presented in this paper. The scheme is performed with a modified readout circuit chip. The shift registers of readout circuit are modified to have the ability to perform parallel test. A full row (or column) of cells can be tested in parallel at the same time. From the test results of rows and columns a faulty cell can be easily identified. Applying the proposed cross-check test scheme, the testing time can be speeded up from the order of M*N to M+N.

To verify the proposed cross-check test scheme, we had designed a 4*4 FPA readout circuit by using UMC 0.5um 2P2M CMOS process. The verification had proven that the proposed cross-check test scheme works out well.

References

[1] F. J. Crawford, "Electro-Optical Sensors Overview," IEEE Aerospace and Electronics Systems Magazines, Oct. 1998, pp.17-24.

[2] N. Itoh, K. Yanagisawa, T. Ichikawa, K. Tarusawa, and H. Kataza, "Kiso observatory near-infrared camera with a large format array," *in Proceedings of the SPIE, infrared technology XXI*, vol. 2552, pp. 430-437, 1995.

[3] D. A. Scribner, M. R. Kruer, and J. M. Killiany," Infrared focal-plane array technology," in *Proc. IEEE*, vol. 79, no.1, pp. 66-85, 1991

[4] E. R. Fossum and B. Pain," Infrared readout electronics for space science sensors: state of the art and future directions," *in Infrared Technology XIX*, Proc. SPIE 2020, pp. 262-285, 1993.

[5] Partrick J. Terado, Ira W. Levin, and E. Neil Lewis, "Indium antimonide(lnSb) Focal Plane Array (FPA) Detection for Near-Infrared Imaging Microscopy", Applied, Spcctroscopy Vol. 48(5), pp.607-615(1994)

[6] Ilan Bloom and Yael Nemirovsky," Quantum Efficiency and Crosstalk of an Improved Backside-Illuminated Indium Antimonide Focal-plane Array", IEEE Transactions on Electron Devices. Vol.38, No.8, pp.1792-1796 (1991).

[7] Ilan Bloom and Yael Nemirovsky, "Bulk Lifetime Determination of Etch-Thinned InSb Wafers for Two-Dimensional Infrared Focal Plane Array", IEEE Transactions on Electron Devices, Vol.39, NO.4, pp.809-812 (1992).

[8] Dean A. Scribner, Melvin R. Kruer, and Joseph M. Killiany, "Infrared Focal Plane Array Technology" Proc. the IEEE, 79(1), pp.66-86 (1991).

[9] C. C. Hsieh, C. Y. Wu, F. W. Jih and T. P. Sun , "Focal Plane Arrays and CMOS Readout Techniques of Infrared Imaging Systems," IEEE Trans. on Circuits and Systems for Video Technology, Aug. 1997.

[10] C. Y. Wu, C. C. Hsieh, "New Design Techniques for a CMOS Current Readout Integration Circuits for Infrared Detector Arrays," Opt. Engineering, Jan. 1995.

[11] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun and Horng Chang , "A New CMOS Readout Circuit Design for the IR FPA with Adaptive Gain Control and Current Mode Background Suppression" IEEE Proc. ISCAS'96, 1996.

[12] C. C. Hsieh, C. Y. Wu and T. P. Sun, "A New Cryogenic CMOS Readout Structure for Infrared Focal Plane Array," IEEE Journal of Solid-State Circuits, Aug. 1997, pp1192-1199.

[13] C. C. Hsieh, C. Y. Wu, T. P. Sun, F. W. Jih and Y. T. Cherng, "High Performance CMOS Buffered gate Modulation Input (BGMI) Readout Circuits for IR FPA," IEEE Journal of Solid-State Circuits, Aug. 1998, pp1188-1198.

[14] M. W. Ng, Y. H. Chee and Y. P. Xu, "On-Chip Compensation of Dark Current in Infrared Focal Plane Arrays," ISCAS 2001, III-509~512.

[15] F. F. Sizov, Yu. P. Derkach, Yu. G. Kononenko and V. P. Reva, "Testing of a Read-Out Device Processing Electronics for IR Linear and Focal-Plane Arrays," SPIE 1998, pp.942~948.

[16] P. J. Thomas et al., "Offset and Gain Compensation in an Integrated Bolometer Array," SPIE 1999.

[17] T. Breen, N. Bulter, M. Kohin, C. A. Marshall, R. Murphy, T. Parker and R. Silva, "More Applications of Uncooled Microbolometer Sensors," SPIE 1998, pp.530~540.

[18] H. Jerominek, T. D. Pope, C. Alain, R. Zhang et al., "128x128 Pixel Uncooled Bolometric FPA for IR Detection and Imaging," SPIE 1998, pp.585~592.

[19] R. Hornsey, P. Thomas, A. Savchenko and T. Pope, "Nonoptical Charactetization Techniques for Uncooled Microbolometer Infrared Sensors," IEEE Trans. on Electron Devices, Dec. 2000, pp.2294~2300.

[20] J. Bajaj, "HgCdTe Infrared Detectors and Focal Plane Arrays," IEEE Optoelectronic and Microelectronic Material Devices, 1999, pp.23~31.

[21] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun and Y. T. Cherng, "High Performance CMOS Bufferes Gate Modulation Input (BGMI) Readout Circuits for IR FPA," IEEE JSSC, Aug. 1998.

[22] T. H. Yu, C. Y. Wu, Y. C. Chin, P. Y. Chen, F. W. Jih, et al., "A New CMOS Readout Circuit for Uncooled Bolometric Infrared Focal Plane Arrays," IEEE ISCAS 2000.

[23] Y. P. Xu, X. B. Qian and G. Karunasiri, "Circuit for Microbolometer bias-heating Cancellation," Electronics Letter, Nov. 2000, pp.1993~1994.

[24] M. V. S. Ramakrishna, G. Karunasiri, P. Neuzil, U. Sridhar and W. J. Zeng, "Highly Sensitive Temperature Sensor using Self-Heating Compensated Microbolometers," Sensors Actuators 2000, pp.122~127.

[25] M. L. Sheu, T. P. Sun and F. W. Jih, "Test Socket Chip for Measuring Dark Current in IR FPA," 1st International Workshop on Electronic Design, Test & Applications (DELTA 2002).