# Measurement of Dark Current of Infrared Detector in Focal Plane Array

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**Abstract:** A circuit chip for measuring the dark current of infrared (IR) detectors in a focal plane array (FPA), based on a measuring path construction, is presented in this paper. To cancel the leakage current resulting from OFF-state MOSs tied to the measuring path, a novel scheme adapted to this chip is also demonstrated. Therefore, the characteristic of detector's dark current in the IR FPA can be accurately acquired.

## I. Introduction

The infrared imaging systems has been developed for various applications for use in military, medical and astronomy. Recently, high-resolution infrared (IR) focal plane arrays (FPA) has become a common requirement in many applications. A large array format (like 128x128, 256x256) and small pixel size (like 50umx50um, 30umx30um) are developed to achieve such high-resolution [1-6].

In general, the IR FPA can be divided into two major parts, a detector array and a readout circuit [1,8,9]. A photovoltaic detector based on a InSb P-N junction device[1,3,5], as shown in Fig 1(a), is used to construct the detector array. The I-V characteristic curve of the detector when exposed to IR radiation is shown in Fig 1(b). The larger the illumination, the larger the reverse current. The readout circuit is designed to bias and interface the detector for subsequent signal processing stage. For the issues of cost and compatibility, CMOS VLSI technology is commonly adopted for the readout circuit implementation [8-13]. A flip chip technology [6-7], as shown in Fig 2, is used to compound the IR detector array and CMOS readout chip by indium bumps which are grown on the aligned pixels of both chips.

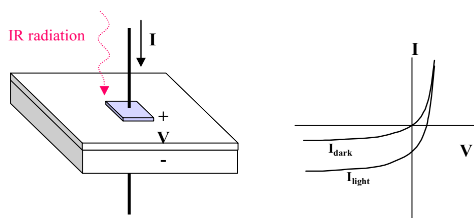



**Fig 1 : A photovoltaic IR detector**

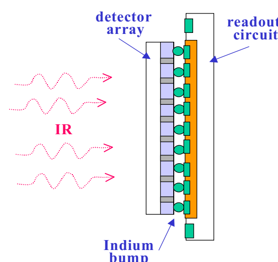



**Fig 2 : A flip-chip by indium bumps**

However, the flip chip process has a high cost. It is necessary to have a qualify examination on the detector array to ensure a high yield before the flip chip process. A characteristic parameter of the IR detector suitable for being examined is the dark current when there is no IR radiation on the detector. As depicted in Fig 1(b), the dark current ($I_{dark}$) must be as small as possible for a good dynamic performance of detectors. A large $I_{dark}$ will lessen the performance of the detector as well as the normal operation of the readout circuit. Hence, it is a must to characterize the dark current of detectors to predict the yield of the detector arrays manufactured in the same batch.

In this paper, a proposed circuit for measuring the dark current of detectors in an IR FPA is presented. The architecture of the circuit is a two-dimension memory-like structure. Each detector is selected by a row address and a column address which control a number of MOS switches to construct a measuring path connecting the addressed detector to an external I/O pad. A reverse bias voltage is applied to the selected detector through this measuring path. A resulting dark current is then measured. However, there exist many OFF-state MOS switches tied to the constructed path. Each OFF-state MOS contributes an OFF-state leakage current, $I_{OFF}$, to the measuring dark current. To derive the accurate dark current, we demonstrate a novel calibration scheme to cancel these unwanted leakage currents in this paper.

The proposed circuit for measuring dark current in an IR FPA is described in section II. The calibration scheme to cancel the unwanted MOS's OFF-state leakage current is presented in section III. The implementation of the proposed circuit for measuring dark current and its associate calibration scheme are unveiled in section IV. Finally, a conclusion is given in the last section.

## II. The Circuit for Measuring Dark Current

The detector in an IR FPA is basically a PN photovoltaic diode. Its I-V characteristic with and without IR radiation is shown in Fig 1(b). It is likable to know the dark current of the diode to quantify the detector's performance. In general, for an InSb IR diode, the dark current is in the range about several pA to a hundred pA under applying a reverse bias of 250mV. The smaller the dark current, the better performance the detector will be. And if the dark current is out of the range, then the detector will be useless. To measure the dark current, it can be directly measured by probing at the bump pad of the detectors. However, the direct probing method needs expensive equipment and time consuming operations. Besides, the uncertainty of the probing contact and interference from the open environment would both make the measurement being more difficult.

To overcome those difficulties, a dark current measurement circuit chip is proposed. This chip compound with the detector array via the aligned bump pad can inherently segregate and reduce the environment interference. The proposed circuit architecture is shown in Fig 3. It resembles the addressing of random access memory. Each

detector in the FPA will be directly accessed through the address lines. When addressed, it will construct a measuring path connecting the selected detector to an I/O pad through a series of NMOS operated at ON-state, as shown in Fig 4. A set of swept reverse bias steps is applied into the addressed detector through the constructed path to measure the dark currents for each voltage step respectively. Therefore, the I-V characteristic of dark current is measured.

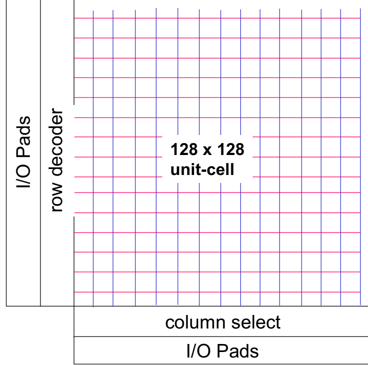



**Fig 3 : The architecture of the testing circuit**

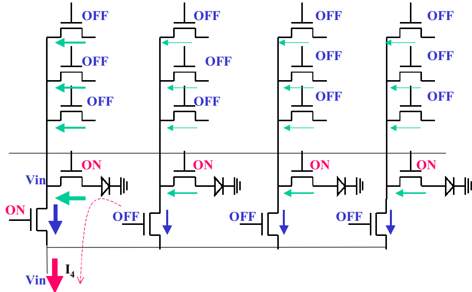


**Fig 4 : The selection of a detector**

Since the dark current, for InSb IR diode, is in the range of about several pA to a hundred pA, the voltage drop along the measuring path according to the parasitic resistance and MOS's ON-resistance, $R_{ON}$, can be neglected, when comparing with the applied reverse bias in a step of 50mV. Nevertheless, there will be a lot of MOSs at OFF-state, the number depended on the array size, tied to the measuring path. All these OFF-state MOSs will contribute a small OFF-state leakage current, $I_{OFF}$, to the path, and totally will have an fairly influence on the measuring result. Hence, it is desirable to calibrate these unwanted leakage currents to derive the accurate value of the detector's dark current. A novel calibration scheme to remove the leakage current of OFF-state MOSs is proposed and demonstrated in the next section.

## III. The Calibration Scheme for the MOS OFF-state Leakage Current

Due to the leakage current of OFF-state MOSs tied to the constructed path for measuring dark current of selected detector, the measured current will have a large error when the array size increased. To calibrate these unwanted leakage current to derive the accurate dark current of the selected detector, by slightly modifying the address decoder, we propose a scheme for calibration of the leakage current.

Since the detectors are arranged in a two dimensional array. A row address and a column address are needed to select a detector via the control of MOSs along the path. To control the state of the MOSs, we use two extra control I/O pins to disable the address selection. That is, even the address has been applied, the output of the selected decoder is still disable. Hence, there will have four cases for the two control inputs. The four cases are shown in Fig 5. The case 1 is that both the addressed row and column are disable. Then all the MOSs are at OFF-state. The case 2 is that the addressed row is disable while the addressed column is still enable. Therefore, only the addressed column MOS is ON and all other MOSs are OFF. The case 3 is that the addressed row is ON and the addressed column is OFF. Thus, all the MOSs at the addressed row are ON, while all other MOSs are OFF. The case 4 is the normal selection. Both the addressed row and column are not disable. Hence, all the MOSs along the addressed row are ON, and the MOS of the addressed column is ON. By measuring the current under these four conditions, we can calibrate the leakage current and derive the accurate dark current of the addressed detector.

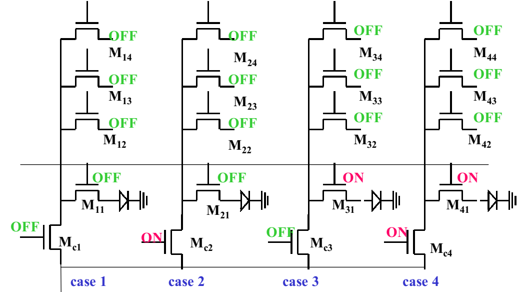



**Fig. 5 : Four conditions of the selection.**

For the four conditions, we will take a close look in the following paragraphs. (Without loss of generality, we assume the numbers of rows and columns are both 4)

**Condition 1**: Both the addressed row and column are disable, as shown in Fig 6. All MOSs are at OFF-state, the measured current, $I_1$, will be the sum of current flowing through the 4 columns of OFF-state MOSs. For each column, the current flowing through the column MOS is the sum of the 4 $I_{OFF}$ of the MOSs tied to this column. Hence, the current flowing at each OFF column MOS is $I_{Mc1} = I_1/4$ .

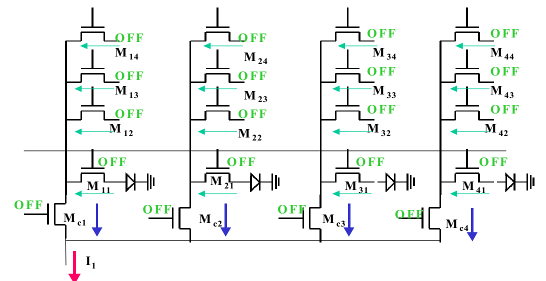



**Fig 6 : The condition 1**

**Condition 2**: The addressed row is disable, and the addressed column MOS is ON. The other MOSs in the array are OFF except the addressed column MOS, as shown in Fig 7. The measured current, $I_2$, is the sum of the current flowing through the addressed column MOS and the other 3 column MOSs at OFF-state. The current flowing through the 3 OFF-state MOSs is the sum of 4 OFF-state MOSs tied to the respective column line. It is the same as condition 1. While for the ON-state column, the applied reverse voltage appears at the column line, although the 4 MOSs tied to this addressed column are all at OFF state, they have different voltage bias from the case 1. The OFF-state MOSs will have a little larger leakage current than those of in condition 1.

Hence, the current flowing at addressed column MOS is equal to $I_2 – (I_1/4)*3$ . And the current flowing at OFF-state MOSs tied to the selected column is equal to $[I_2–(I_1/4)*3]/4$ .

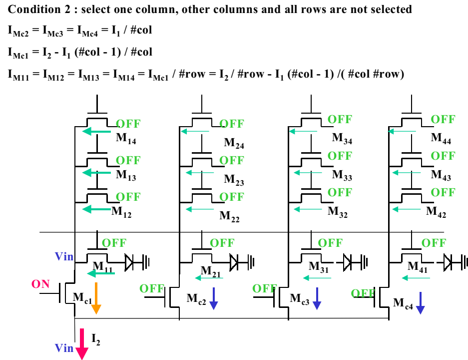



**Fig 7 : The condition 2**

**Condition 3**: The addressed column is disable while the addressed row is selected. All the column MOSs are at OFF-state, and the addressed row MOSs are at ON-state, as shown in Fig 8. The 4 MOSs of the selected row are at ON state and the others are at OFF state. The measured current, $I_3$, is the sum of 4 OFF-state column MOSs. For each column MOS, the current is the sum of 3 OFF-state MOSs and one ON-state MOS. (Notice that: since the row is selected, the dark current of the detector will flow through the ON-state MOS to charge the column line, and change the bias of the MOSs tied in the column. Hence the $I_{OFF}$ is different from those of condition 1 and 2.) All 4 column MOSs have the same bias, then the current flowing at column MOS is equal to $I_3/4$ .

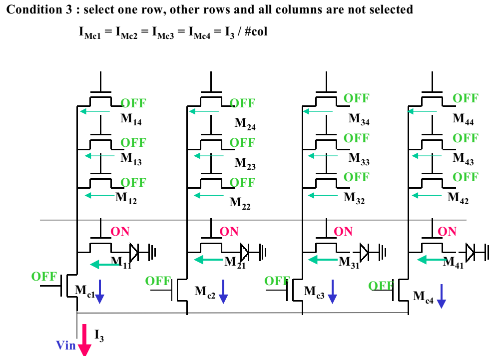



**Fig 8 : The condition 3**

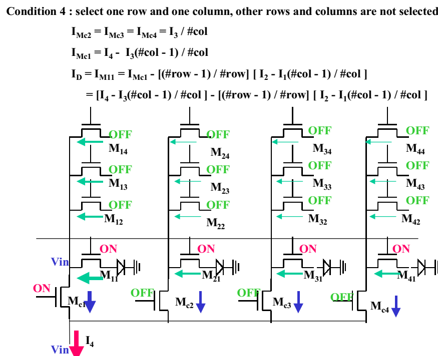



**Fig 9 : The condition 4**

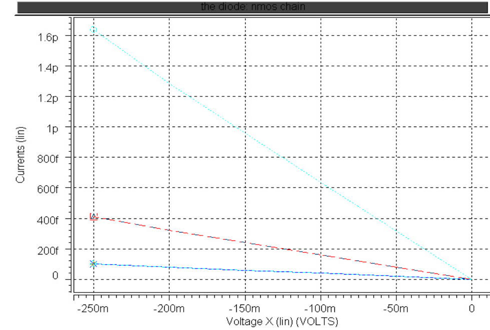
**Condition 4**: It is the normal selection. Both the addressed row and column are selected. The selected column MOS and the row MOSs are at ON-state, and other MOSs are OFF, as shown in Fig 9. The measured current, $I_4$, is the sum of 3 OFF-state column MOSs and one ON-state column MOS. For the OFF-state column MOSs, the current is the same as condition 3. For the ON-state column MOS, its curent is the sum of 3 OFF-state row MOSs and one ON-state row MOS. For the OFF-state row MOSs, the current is the same as condition 2. For the ON-state row MOS, its curent is the dark current of detector. Hence, the dark current $I_D = I_4 – 3( I_3/4) - 3[I_2 – (I_1/4)*3] / 4$ .

Based on the relationship of the four measured currents, we can derive the correct detector dark current to be $I_D = I_4 – k_1I_3 – k_2I_2 + k_1k_2I_1$ , where $k_1 = (\#col–1)/\#col$, $k_2= (\#row–1)/\#row$, when #row and #col are large enough, (i.e., $k_1, k_2>>1$), the dark current will close to be $I_4 – I_3 – I_2 + I_1$ .

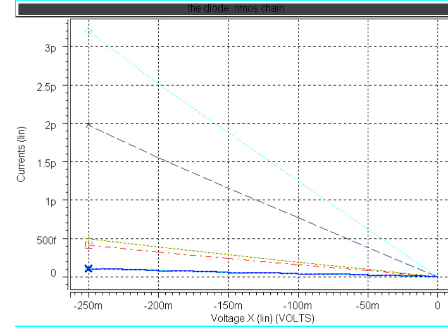
Fig 10 is simulation results of the four conditions for a 4 x 4 array. The corresponding currents are listed at the top for each case.

Case 1:

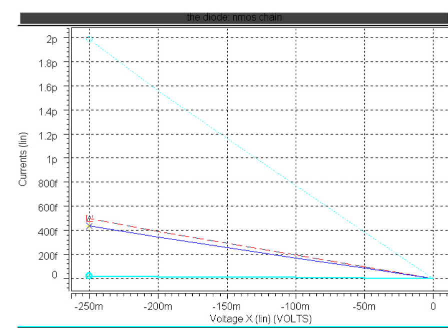
$I_1 = 1.64$, $I_{Mc1} = I_{Mc2} = I_{Mc3} = I_{Mc2} = 0.409$, $I_{M11} = I_{M12} = I_{M21} = … = 0.102$




Case 2: $I_2 = 3.2$ ,
$I_{Mc1} = 1.97$, $I_{M11} = I_{M12} = I_{M13} = I_{M14} = 0.493$,
$I_{Mc2} = I_{Mc3} = I_{Mc2} = 0.409$, $I_{M21} = I_{M22} = … = 0.102$




Case 3: $I_3 = 1.98$ ,
$I_{Mc1} = I_{Mc2} = I_{Mc3} = I_{Mc2} = 0.496$ , $I_{M11} = I_{M21} = I_{M31} = I_{M41} = 0.438$,
$I_{M12} = I_{M13} = I_{M14} = I_{M22} = I_{M23}$ … = 0.0193




Case 4:
$I_4 = 13.1$ ,
$I_{Mc1} = 11.6$ , $I_{Mc2} = I_{Mc3} = I_{Mc2} = 0.496$ , $I_{M11} = 10.1 = I_D$ , $I_{M12} = I_{M13} = I_{M14} = 0.493$,
$I_{M21} = I_{M31} = I_{M41} = 0.438$, $I_{M22} = I_{M23}$ … = 0.0193

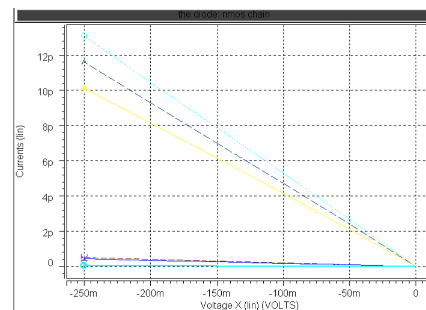



**Fig 9 : Simulation of 16x16 Array**

## IV. Implementation

For a 128 x 128 IR FPA, the unit cell is of the size 30um x 30um. The unit cell includes 3 NMOS switches, a small size P+_N-Well diode for testing purpose, and a bump pad. Fig 10 and 11 are its schematic and layout. To verify the circuit before bump, a control signal, *test*, is used to select the testing diode in the unit cell. A forward bias voltage is then applied on the testing diode to verify the address decoder's function. After bump, the path is switched to bump-pad where the IR detector attached, then the dark currents are measured according to the calibration scheme described in section III. The layout for 128 x 128 IR FPA testing circuit is shown in Fig 12. It has been submitted to the MPC service of CIC. The technology used is UMC 0.5um 2P2M CMOS process. The chip size is 4518 um x 4364 um.

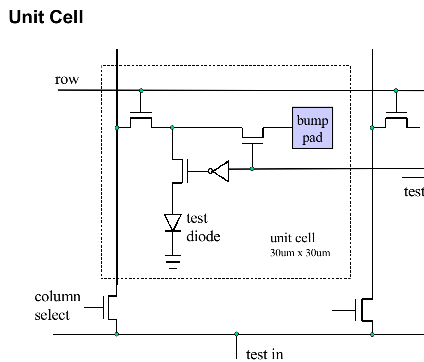



**Fig 10 : The schematic of a unit cell**

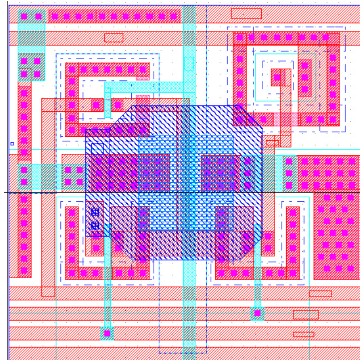


**Fig 11 : The layout of a unit cell**

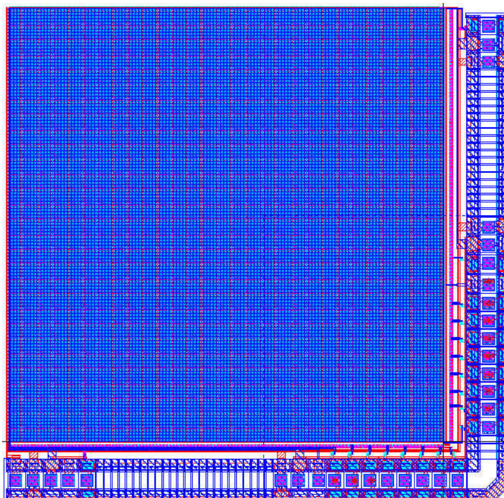


**Fig 12 : The circuit for dark current measurement in 128 x 128 IR FPA**

## V. Conclusion

A circuit chip for the measurement of dark current of IR detector in a FPA is presented in this paper. The chip employed a proposed calibration scheme to remedy the leakage current of OFF-state MOSs. Hence, an accurate I-V characteristic of detectors can be constructed. The resultant characteristics of the whole array can be used to construct a failure map and predict the gross yield before bump.

The circuit chip had been submitted to CIC for fabrication using UMC 0.5um 2P2M process. The fabricated and verified testing chip will be interfaced with a PC to establish an automatic measuring system which is now under developing at Department of Electrical Engineering, National Chi Nan University.

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