THE FAULT DETECTION OF CROSS-CHECK TEST SCHEME FOR INFRARED FPA

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ABSTRACT

The increase of array size and decrease of cell size make the testing of infrared focal plane array (FPA) being difficult. A design for test scheme, cross-check test, for infrared focal plane array (FPA) is presented in this paper. For an array size of M by N, the testing times can be reduced from the order of M*N to M+N. Analysis on the fault detectability of the proposed test scheme is also presented in this paper.

Keywords: FPA, Cross-Check Test, Readout, Fault Model

1. INTRODUCTION

Recently, large array format and small pixel size are indispensable to achieve high-resolution infrared (IR) focal plane array (FPA) applications for uses in military, medical and astronomy [1-4]. In general, an IR FPA consists of a sensor array and a readout circuit [5]. The sensor array is constructed by a two-dimensional array of photovoltaic detectors whose I-V characteristic curve resembles a photo diode. The readout circuit is designed to provide an interface between the detectors and subsequent signal processing stage. Taking into account of cost and compatibility, the readout circuit is commonly realized by using CMOS technology [6-8]. The readout circuit and the sensor array chips are then compounded face to face by flip chip technology [4-5], as shown in Fig. 1.

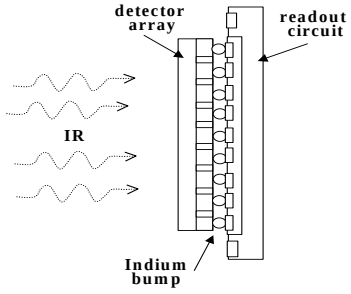


Figure 1. A flip-chip binding

The increase of array size and decrease of cell size will unavoidably increase the possibility of defect occurrence during manufacturing and flip chip process. Technologies of nowadays can easily achieve an array size of 256 by 256, and cell size of 20μm by 20μm. Hence, it is urgent to include a design for test scheme to economically test the detector array and readout chips of a large size FPA. To test the readout circuit, extra current sources built in the readout circuit itself to substitute for the function of sensor cell during testing had been proposed [9-13]. To test the sensor array before the flip chip process, the sensor cell can be probed directly for measuring its I/V characteristic [15]. Nevertheless, the total probe time will be proportional to the array size and become unacceptable when the array size grows large. Beside that, the probe contact for small cell size will impose the uncertainty of the measured results. In [16], a modification on the cell selection in FPA had been proposed to calibrate the dark current by a series of measurements at different selection modes. All the above methods test a cell each time. Hence, for an array size of M by N, at least M*N times of testing are required to test all cells once. In order to reduce the total number of testing times, a parallel test scheme, called cross-check test, was proposed and presented in [17]. Column by column and row by row, parallel test is performed with a modified cell selection maneuver. As a result, the testing times can be reduced from the order of M*N to M+N. In this paper, the cross-check test scheme for FPA is reexamined in section II. Based on the test scheme, a fault model and its detectability are unveiled in section III. Finally, the work is summarized in the last section.

2. THE CROSS-CHECK TEST SCHEME

A readout circuit for FPA is shown in Fig. 2. It consists of a row decoder, a column selector, and a two-dimensional array of unit cells for sensor readout. The unit cell, as depicted in Fig. 3, contains a bump pad for sensor binding, a readout circuit, and a row-select MOS switch. Each sensor cell in the FPA will be sequentially scanned through the addressing operations on row and column selection lines. The row decoder and the column selector are generally implemented by shift register, as shown in Fig. 4. The shift register is basically a cyclic one with load, clear and preset functions. In normal operation, only one DFF in row shift register and one DFF in column shift register are set to activate the row and column MOS switches respectively. Hence, a row is selected and a cell in the selected row is addressed, as shown in Fig. 5. The other cells in the selected row are sequentially addressed, then follow through the cells of the other rows.

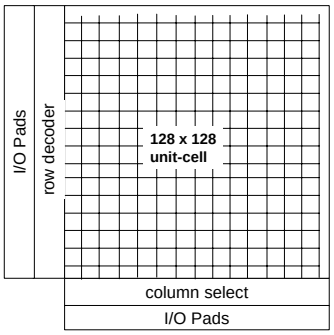


Figure 2. The architecture of the readout circuit

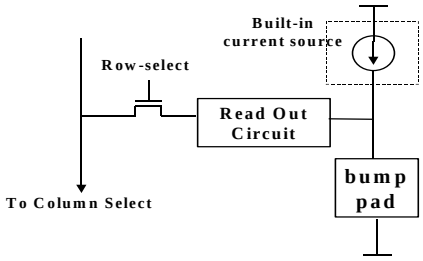


Figure 3. The unit cell of readout circuit

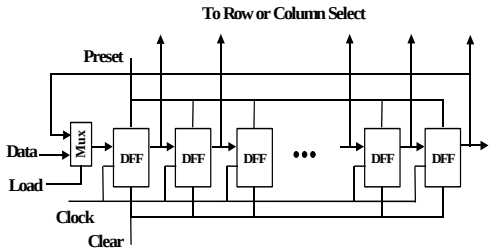


Figure 4. The shift register

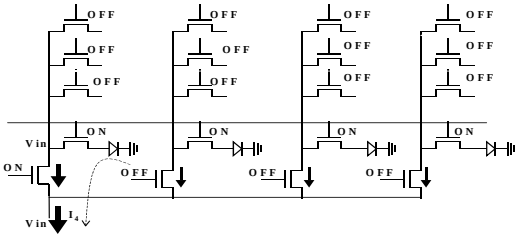


Figure 5. The normal selection of a detector

Before the flip chip binding, the bump pad is floating; hence the readout circuit can not operate functionally and be tested. A possible testing method is to include a current source, as shown in Fig. 3, attached to the bump pad. The function of photo-sensor will be replaced, during testing, by the built-in current source that can provide a current to the readout circuit.

To test a FPA of large array size, conventional methods need at least M*N times of test to exercise all cells (without loss of generality, we assume that M is the number of columns and N is the number of rows). When the array size grows large, the number of test times becomes unacceptable. In order to reduce the number of test times, resemble the idea proposed in [16], a parallel test scheme, called cross-check test, is proposed in [17]. As a result, the number of test times can be thus reduced from the order of M*N to M+N.

To perform cross-check test, the shift register in readout circuit must have the functions of clear/preset and load. The shift register shown in Fig. 4 can perform these functions. With these functions, the stored pattern in the shift register can be controlled. In normal operation, each time, only one row and one column are activated, that is, only one DFF in the shift register can be ON. To perform a parallel test, it demands that all rows and all columns can be intentionally selected to be ON. Hence, we can select all rows or all columns for parallel test. That is, for example, if a full row of cells are needed to be tested in parallel, the DFF for the tested row in row shift register should be ON, and all the DFFs in column shift register should be ON, as shown in Fig. 6. It is similar to parallel testing a full column, as shown in Fig. 7.

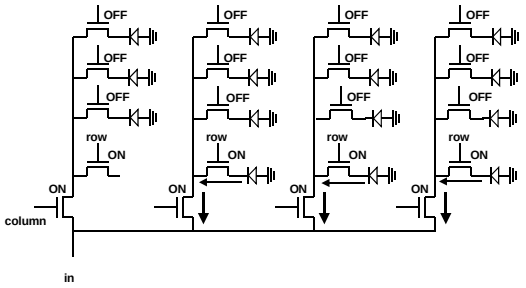


Figure 6. The selection of one full row

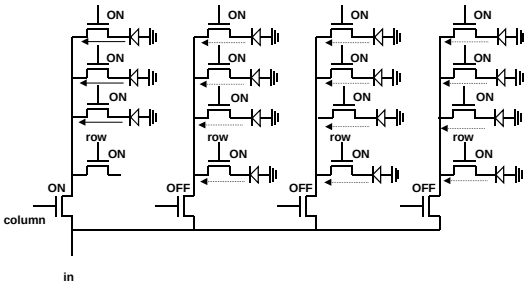


Figure 7. The selection of one full column

The cross-check test scheme is to test a full row of cells in parallel for each row, and followed by a full column of cells in parallel for each column. Consequently, row by row and column by column, the number of test times is reduced to M+N. The steps for cross-check test are as follows:

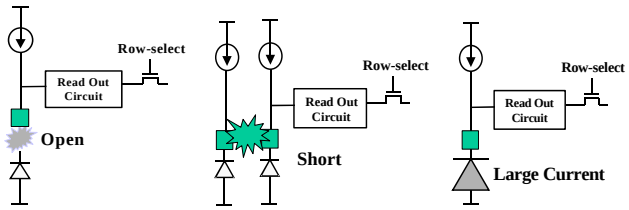
(1) For each row, measure the total currents of one full row. As shown in Fig. 6, all columns are selected to be ON, and only the interested row is selected to be ON. Sensors in the interested row will contribute their currents to the measurement. Therefore, if there is no faulty sensor cell in the row, the measured current will be M times of one cell's. And if there are faulty cells, the measured current will be different from the expected value.

(2) For each column, measure the total currents of one full column. As shown in Fig. 7, all rows are selected to be ON,

and only the interested column is selected to be ON. Sensors in the interested column will contribute their currents to the measurement. Therefore, if there is no faulty sensor cell in the column, the measured current will be N times of one cell's. And if there are faulty cells, the measured current will possibly be different from the expected value.

From the measurement results of the above two steps, we can cross check them to identify which cell is faulty. For example, if cell (i,j) is faulty, then the measurements of i^{th} column and j^{th} row will reflect this fault.

With the built-in current source, as shown in Fig. 3, the readout circuit can be tested before the binding of readout and sensor array chips. After binding, the cells in sensor array can be tested by measuring their dark currents. If the cells are tested one by one, the number of testing times will grow into unacceptable when the array size become large. Hence it is desirable to employ parallel test scheme. Cross-check test can perform parallel test, however, there does exist possibility of fault masking. In the next section, we will categorize the possible faults and figure in the fault detectablility of cross-check test.



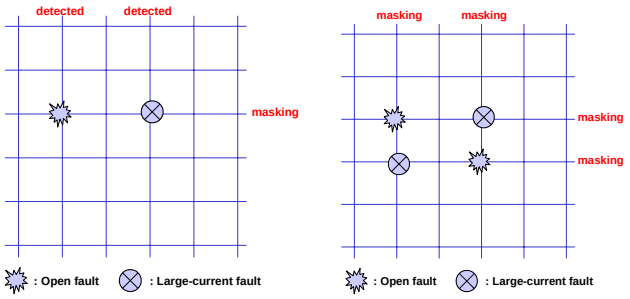
(a) (b) (c)

Figure 8. (a) open fault, (b) short fault, (c) large-current fault

3. FAULT DETECTABILITY OF CROSS-CHECK TEST

Since the testing is mainly relying on the measurement of current, it is convenient to classify the possible occurring faults, after binding of readout and sensor array chips, into three categories: open fault, short fault and large-current fault, as illustrated in Fig. 8. The open fault, as shown in Fig. 8(a), is caused by an unhealthy binding where the bumps between readout and sensor array chips are not connected. Therefore the bump pad of the readout is floating and no current appears. The short fault, as shown in Fig. 8(b), is also caused by an unhealthy binding where the adjacent bumps are shorted together. Consequently the shorted cells will receive extra currents from each other. The large-current fault, as shown in Fig. 8(c), is caused by bad sensor cell that has a large leakage current. The short fault can be regarded as a type of large-current fault. For simplicity, we will only treat the open fault and large-current fault in subsequent analysis. If the cells in FPA are tested by individually measuring their currents, the open fault and large-current fault can be obviously detected and located. Yet if they are tested by cross-check test in parallel, there does exist possibility of fault masking.

When only single-fault model is considered, there exists no fault masking. All single-fault can be evidently detected and located by cross-check test. When double-fault model is considered, if only one fault type is allowed, say open fault or large-current fault, then both faults of double-fault can be detected and located. However, if both open and large-current fault types are allowed, then both faults can be detected yet not located in some case. For example, as shown in Fig. 9(a), an open fault and a large-current fault whose current is doubled exist in a same row. In this case, when performing cross-check test, testing row by row can not identify the faulty row due to current cancellation of the two faults. Nevertheless, testing column by column can identify the faulty columns that the two faults belong to. It is similar that when double-fault exists in a same column. If the two faults of double-fault do not exist in the same row or same column, both faults can be detected and located by cross-check test. When higher level of multiple-fault is considered, the possibility of fault masking will increase. And if the faulty cells canceling each other currents by row and column in the same time, then there will be no fault detected, as shown in Fig. 9(b) for a quadri-fault case.



(a) (b)

Figure 9. (a) A double-fault. (b) A quadri-fault.

To verify the proposed cross check test scheme, a test chip of readout circuit for 4x4 array, as shown in Fig. 10, is fabricated by using UMC 0.5μm 2p2m CMOS process. A current source is built in with each cell of the array. The measurement results for the array are shown in Table 1-4. For these tables, we have first probed each cell to measure the current of its own current source, as recorded in the middle part of the tables. Then follow the cross check test on rows and columns of the array. In the table, the last column records the parallel test of each row, and the last row records the parallel test of each column. To inject an open fault, a laser cutter is employed to cut the connection line between the current source and cell. To inject a short fault, the intentionally connect line between two adjacent cells is left uncut, while it is cut for the good one case.

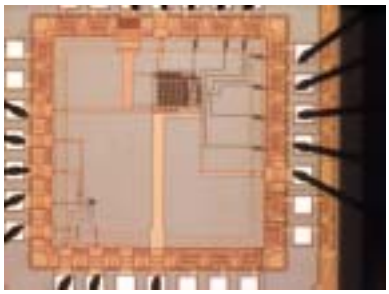


Figure 10. A readout circuit for 4x4 array.

Table 1 is the good one case. The cross check test of rows and columns are evident that there does not exist fault in the array. Table 2 is demonstrating an open fault on cell(3,2). The cross check test results of row-3 and column-2 smaller than others exhibit the open fault. Table 3 is the short fault case between cell(4,3) and cell(4,4). The column-3 and column-4 results are larger than normal one to show that exists a short fault between column 3 and 4. However, the row-4 result, due to fault masking, can not distinguish from others. Table 4 is a double-fault case, where an open fault on cell(3,2) as well as a short fault between cell(2,1) and cell(3,1) are injected. A fault masking is occurred at the row-3 test.

4. SUMMARY

To reduce the number of test times of FPA in large array size, a parallel test scheme, called cross-check test, is proposed and presented in this paper. A full row (or column) of cells can be tested in parallel at the same time. By cross checking the test results of rows and columns a faulty cell can be easily identified. Applying the proposed cross-check test scheme, the number of testing times can be speeded up from the order of M*N to M+N. The fault detectability of cross-check test is analyzed based on proposed fault model for FPA. Single fault can be fully detected and located. Double-fault can be detected yet not located in some case. Higher level of multiple-fault can result fault masking hence reduce the detectability of cross-check test.

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Table 1 : good

	1	2	3	4	row
1	0.95	0.94	0.92	0.94	3.78
2	0.96	0.95	0.93	0.95	3.83
3	0.94	0.94	0.95	0.94	3.81
4	0.97	0.96	0.95	0.96	3.87
col	3.88	3.84	3.80	3.81	

Table 2 : open fault

	1	2	3	4	row
1	0.96	0.96	0.92	0.95	3.81
2	0.96	0.96	0.92	0.94	3.82
3	0.95	**0**	0.94	0.95	**2.88**
4	0.98	0.95	0.93	0.95	3.85
col	3.90	**2.92**	3.79	3.83	

Table 3 : short fault

	1	2	3	4	row
1	0.96	0.94	0.93	0.95	3.81
2	0.96	0.94	0.94	0.95	3.83
3	0.95	0.94	0.95	0.95	3.82
4	0.96	0.95	**1.92**	**1.92**	3.89
col	3.90	3.82	**5.01**	**5.02**	

Table 4 : open + short faults

	1	2	3	4	row
1	0.95	0.94	0.93	0.95	3.79
2	**1.91**	0.95	0.93	0.95	**4.81**
3	**1.91**	**0**	0.95	0.94	**3.83**
4	0.96	0.95	0.94	0.95	3.85
col	3.89	**2.90**	3.81	3.84	

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