A 1.5V 5.2GHz LNA in 0.25um CMOS Utilizing Inter-Stage Matching

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ABSTRACT

In this paper, a 5.2GHz low noise amplifier in 0.25um CMOS utilizing inter-stage matching is designed. Two realizations for a low value of inductor within the LNA are implemented. The measurement results are 7dB gain and 5.86dB noise figure is achieved for the on-chip inductor realization, and 8.3dB gain and 5.74dB noise figure is achieved for the bond-wire inductor realization.

Keywords: low noise amplifier, inter-stage matching, cascode, inductive degeneration

1. INTRODUCTION

Due to the rapid advance in technologies, the products of wireless communication have boosted to dramatically shorten the connections between people. In addition to the voice connection, the demands for audio, video, and multimedia data accessing have embarrassed the limited bandwidth. To fulfil the growing demands for high bandwidth wireless connectivity, IEEE ratified in 1999 two wireless networking communications standards, dubbed 802.11a (for operation at 5GHz) and 802.11b (at 2.4GHz) [1].

The continuous advance of CMOS process technology, which is low cost and highly integrated, has evidenced the widely growing applications in RF front-end circuits [2]. Recently, a large number of efforts have been reported to use the advanced CMOS process for single-chip implementation of a complete RF transceiver. In the receiver of the RF front-end circuits, low noise amplifier (LNA) is the first active element in the receiver chain, and plays a significant role in the overall noise figure (NF) of the receiver. LNAs using cascade topology had been demonstrated in [3,4], and LNAs using cascode configuration were presented in [5,6,7]. Significant progress in CMOS LNA design has been made during the last several years, shows that CMOS LNAs can be a worthy competitor for compound semiconductor process.

In this paper, a 5.2GHz low noise amplifier in 0.25um CMOS utilizing inter-stage matching is designed. A series inductor seated between the common source and common gate stages of a cascode amplifier is used for the inter-stage matching. The inter-stage matching will help the power transfer to benefit the gain and signal-to-noise ratio. Two implementations for the low value of degeneration inductor in LNA are realized and measured. The measurement results are 7dB gain and 5.86dB noise figure is achieved for the LNA employing on-chip inductor, and 8.3dB gain and 5.74dB noise figure is achieved for the LNA employing bond-wire inductor.

2. DESIGN OF LOW NOISE AMPLIFIER

2.1 Noise Model

For a common source input stage in a low noise amplifier, as shown in Fig. 1, the main noise source comes from transistor M1. By using the noise model of transistor derived in [2], the noise model of the common source stage is also illustrated in Fig. 1. The noise factor can be expressed as :

$$F = 1 + \frac{R_l}{R_s} + \frac{R_l}{R_s} + \frac{\gamma}{\alpha}\frac{\omega_0}{\omega_T} x \qquad (1)$$

$$\alpha = \frac{g_{m1}}{g_{d0}}$$

$$x = \frac{1 + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}}{Q_L} + \frac{\delta\alpha^2}{5\gamma} Q_L$$

$$Q_L = \frac{\omega_0 (L_s + L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}}$$

From the above equations, the noise figure is related to Q_L, while Q_L is inverse proportional to C_{gs} whose value is determined by transistor size.

To trade-off between the noise figure and power consumption in the design of low noise amplifier, a plot of noise figure versus Q_L under different power consumptions is demonstrated in Fig. 2 based on the above equations. As the plot reveals that the noise figure has a minimum value when Q_L is nearby 5. And both larger QL (smaller transistor size) and smaller QL (larger transistor size) will make the noise figure be larger. Also, the more the power consumption, the smaller the noise figure we get.

2.2 Inductive Degeneration

In a common-source LNA, inductive degeneration is used to generate the real part needed to match the LNA input to the preceding antenna or filter. As shown in Fig. 1, two inductors, L_s and L_g, are placed at the source and

gate terminals of the input transistor, respectively. Hence, the input impedance can be expressed as :

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \qquad (2)$$

$$\cong \omega_0 L_s = 50\ \Omega, \text{ when } \omega = \omega_0$$

$$\omega_T = \frac{g_{m1}}{C_{gs}} \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}$$

By tuning the values of inductors, real part of impedance can be achieved as 50 Ω while imaginary part be zero.

The inductive degeneration can enhance the output SNR. The ideal lossless inductive feedback moves the source impedance for optimum NF toward the optimum power match with a minor increase in the minimum NF. However, the loss associated with silicon on-chip inductor will degrade the NF. In this case, cascode configuration can be used to enhance the stability and reverse-isolation of the amplifier.

2.3 Cascode Configuration

The LNA design incorporated in a single common-source transistor as the input stage exists a problem. The parasitic capacitor, C_{gd}, which exists between gate and drain terminals of input transistor, provides the output signal a feedback path to input which will cause the instability problem. To dismiss this problem, a cascode circuit structure, as shown in Fig. 3, is used to break the direct path by inserting a common gate stage in the path. C_{gd} of common gate stage will no longer be the Miller effect capacitor. Therefore, the instability caused by feedback path is eliminated. In the figure, L_g and L_s are used for input impedance matching, while L_1, L_2, and C_1 are used for output impedance matching.

2.4 Inter-Stage Matching

There is no impedance matching performed on the common source and common gate stages of a general cascode low noise amplifier [8], as shown in Fig. 3. This will reduce the gain and signal-to-noise ratio. An inter-stage matching inductor, L_m as shown in Fig. 4, seated between the common source and common gate stages, can cancel out the effect of parasitic capacitors, c_{ds1} and c_{gs2}, as illustrated in Fig. 5. Consequently, the power transfer efficiency from M1 to M2 will be increased, and the gain and signal-to-noise ratio will then be improved.

3. CIRCUIT IMPLEMENTATION

To realize a LNA for 5.2GHz band, we choose the 0.25um 1p5m CMOS process of TSMC provided by CIC. The process supports RF model for a library of MOS transistors and inductors. ADS of Agilent is used to run the circuit simulation. The LNA circuit designed is a cascode structure employing inductive degeneration as well as inter-stage matching, as shown in Fig. 4. The values of components are listed in Table 1. However, the degeneration inductor, L_s, has a small value, there is no adequate on-chip inductor provided by the process library. Hence, we adopt two methods to implement this inductor. The first method is shunting three on-chip inductors to have the small value inductor. The second one is using parallel off-chip bond-wire. They are shown in Fig. 6 and Fig. 7, respectively.

4. MEASUREMENT RESULTS

The fabricated chips are measured by on wafer probing with Agilent 8510 vector network analyzer sited on CIC. The four S parameters, noise figure, and -1dB gain compression point are measured for the two different implementations of L_s, respectively. Fig. 8 is the measurement results of shunt on-chip inductor. Fig. 19 are the measurements of parallel bond-wire inductor. Table 2 lists the comparisons of the measurement results. The measurement results have a little worse than the simulation ones. The gain has dropped about 3dB for on-chip inductor and 1.8dB for bond-wire inductor. The noise figure has increased 1.2dB for on-chip inductor and 1.1dB for bond-wire inductor. These losses can be imputed to imperfect models of devices and process variations. Moreover, the impedance matching between the chip and probes were not finely tuned will furthermore cause the losses. Also, the measurement results evidence that the bond-wire inductor outperforms on-chip inductor due to its higher quality factor.

5. CONCLUSIONS

In this paper, a 5.2GHz low noise amplifier for WLAN applications is designed by using 0.25um 1p5m CMOS process. The LNA utilizes a cascode structure with inter-stage matching as well as inductive source degeneration. Two implementations for the low value of degeneration inductor are realized and measured. The measurement results are 7dB gain and 5.86dB noise figure is achieved for the shunt on-chip inductor implementation, and 8.3dB gain and 5.74dB noise figure is achieved for the parallel bond-wire inductor implementation.

Acknowledgement

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Table 1 The component list of cascode LNA

M1	**16x10x0.24**
M2	**32x10x0.24**
L1、Lg	**2.185 nH**
Ls	**0.5 nH**
L2	**3.715 nH**
C1	**225 fF**

Table 2 Comparisons between on-chip

Cascode LNA	Voltage (V)	NF (dB)	Gain (dB)	S11 (dB)	S12 (dB)	S22 (dB)	P_{1dB} (dBm)	Power (mW)
On-chip L	**1.5**	**5.86**	**7**	**-11.5**	**-18.5**	**-10.5**	**-1**	**7.5**
Bond-wire L	**1.5**	**5.74**	**8.3**	**-9.3**	**-16.9**	**-5.9**	**-2**	**7.5**
Simulation	1.5	4.56	10.1	-17.3	-24.4	-27.9	0	4.2

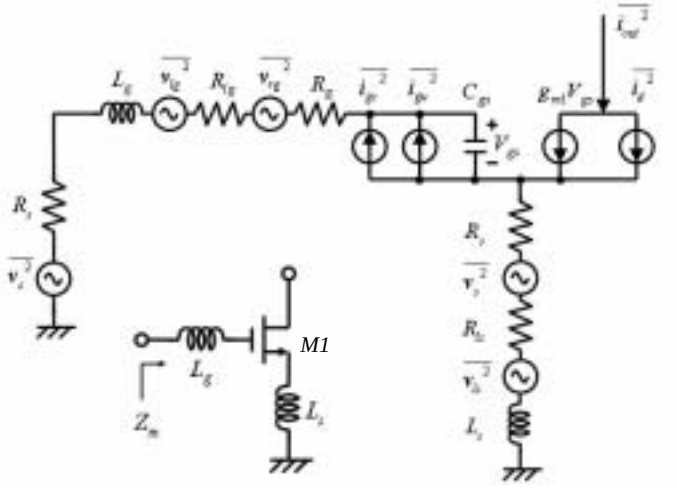


Figure 1 Common-source input stage and its noise model

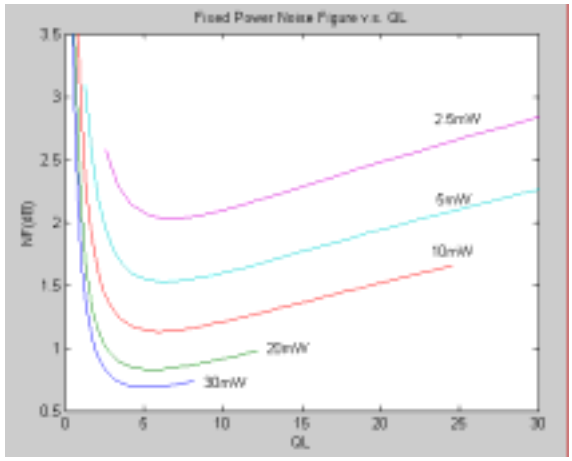


Fig. 2 Noise figure versus Q_L

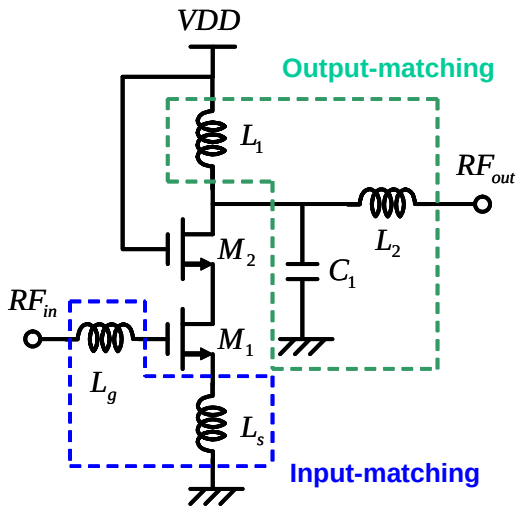


Fig. 3 Cascode LNA

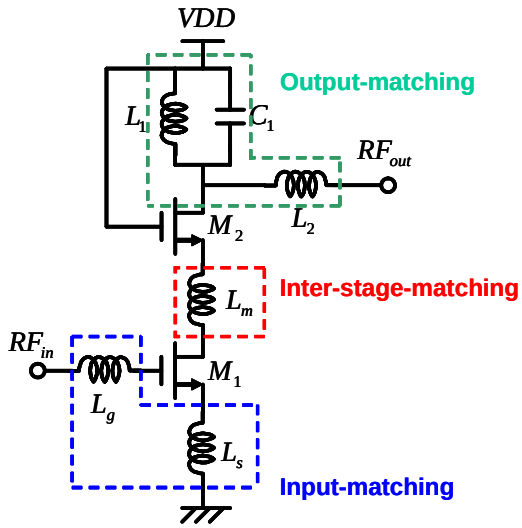


Fig. 4 Cascode LNA with inter-stage matching

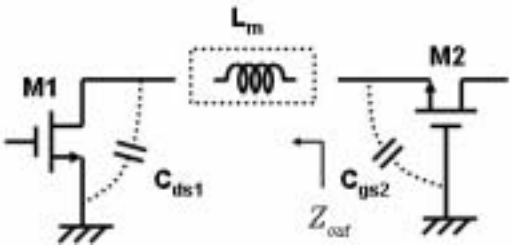


Fig. 5 Inter-stage matching

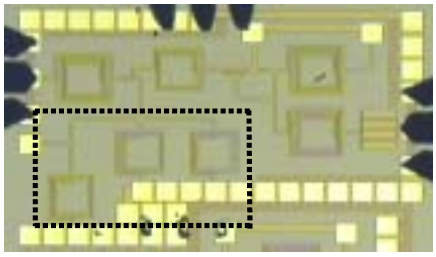


Fig. 6 Shunt on-chip inductor

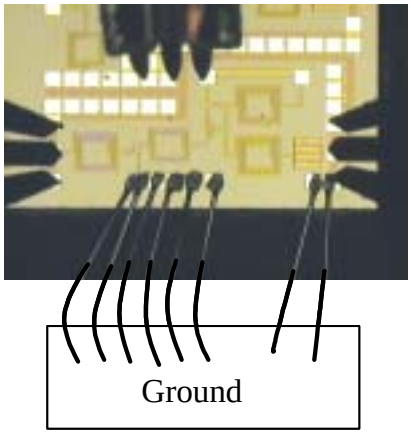
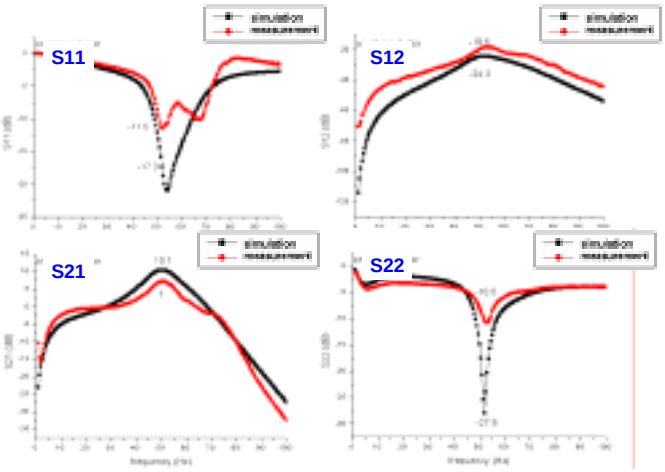
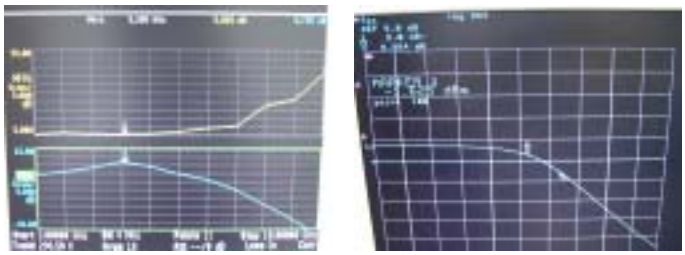


Fig. 7 Parallel bond-wire inductor

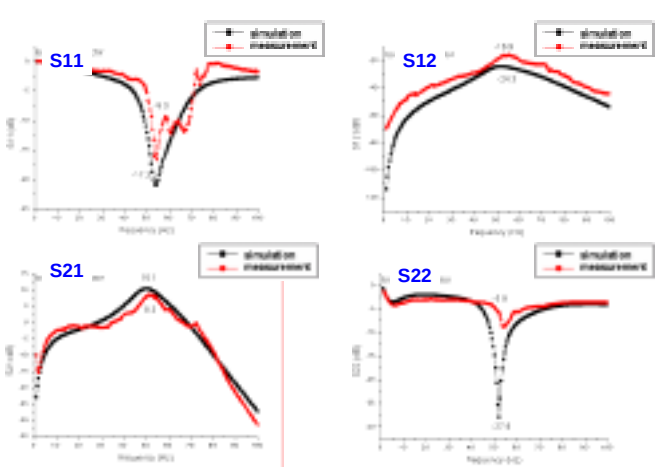


NF=5.86dB P_{1dB}= -1dBm

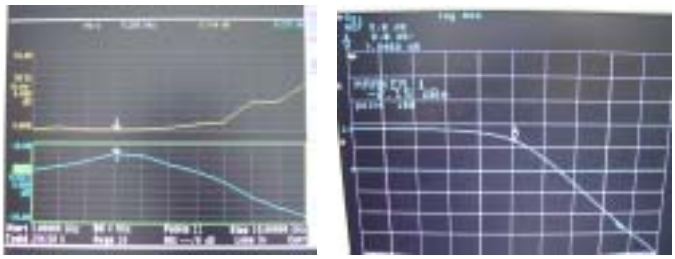


On-chip Inductor	Voltage (V)	NF (dB)	Gain (dB)	S11 (dB)	S12 (dB)	S22 (dB)	P_{1dB} (dBm)	Current (mA)	Power (mW)
Measurment	1.5	5.86	7	-11.5	-18.5	-10.5	-1	5	7.5
Simulation	1.5	4.56	10.1	-17.3	-24.4	-27.9	0	2.8	4.2

Fig. 8 Measurement and simulation results for on-chip inductor LNA



NF=5. 74dB P_{1dB}= -2dBm



Bond-wire Inductor	Voltage (V)	NF (dB)	Gain (dB)	S11 (dB)	S12 (dB)	S22 (dB)	P_{1dB} (dBm)	Current (mA)	Power (mW)
Measurment	1.5	5.74	8.3	-9.3	-16.9	-5.9	-2	5	7.5
Simulation	1.5	4.56	10.1	-17.3	-24.4	-27.9	0	2.8	4.2

Fig. 9 Measurement and simulation results for bond-wire inductor LNA