Test Socket Chip for Measuring Dark Currents in IR FPA

Meng Lieh Sheu, Tai Ping Sun, Far-Wen Jih*

Department of Electrical Engineering
National Chi-Nan University
*Chung-Shan Institute of Science and Technology

Email: sheu@ncnu.edu.tw

Abstract

A test socket chip for measuring dark currents of infrared (IR) detectors in a focal plane array (FPA) is presented in this paper. A calibration scheme adopted in this chip to cancel the leakage current due to OFF-state MOS switches tied to the measuring path is also demonstrated.

Keywords: Test Socket Chip, Infrared(IR), Focal Plane Array(FPA), Dark Current

1. Introduction

Recently, high-resolution infrared (IR) focal plane arrays (FPA) for infrared imaging systems have been developed for various applications including IR search and track, medical examination, astronomy and military. [1-5].

In general, the IR FPA comprises two major parts, a detector array and a readout circuit [1,3,8]. In this paper, the detector to be examined is constructed by InSb P-N junction photovoltaic device [1,3,5], as shown in Fig 1(a). Its I-V characteristic curve, when exposed to IR radiation, is shown in Fig 1(b). A reverse current exists proportionally to the strength of IR radiation. The readout circuit biases and interfaces the detector for subsequent signal processing. For the issues of cost and compatibility, CMOS VLSI technology is usually adopted for the readout circuit implementation [8-12]. An indium-bump flip-chip technology [3,5-7] is used to compound the IR detector array and the readout chip, as shown in Fig 2.

It is necessary to have a quality examination on the detector array to ensure a high yield before the flip-chip process. The dark current, when there is no IR radiation on the detector, is a suitable candidate to be examined. As depicted in Fig 1(b), a small dark current (I_{dark}) means a good dynamic performance of detectors. A large I_{dark} will lessen the performance of the detector as well as the normal operation of the readout circuit. Hence, it is a must to characterize the dark current to predict the yield of the detector arrays.

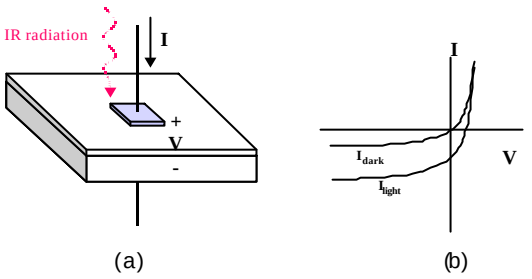


Fig 1 : A photovoltaic IR detector

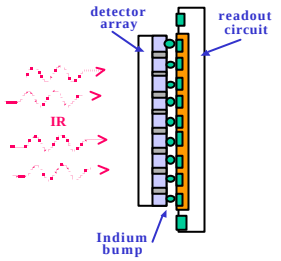


Fig 2 : A flip-chip by indium bumps

In this paper, a proposed test socket circuit chip for measuring dark currents of detectors in an IR FPA is presented. The circuit is a two-dimension memory-like structure. Each detector is selected by a row address and a column address which control a number of MOS switches to construct a measuring path connecting the addressed detector to an external I/O pad. A reverse bias voltage is applied to the selected detector through this path to measure the dark current. However, there are many OFF-

state MOS switches tied to the constructed path. Each OFF-state MOS will contribute an OFF-state leakage current, I_{OFF}, to the measured current. To derive an accurate dark current, we demonstrate a novel calibration scheme to cancel these unwanted leakage currents.

The proposed test socket circuit for measuring dark currents in an IR FPA is described in section 2. The calibration scheme to cancel the unwanted MOS's OFF-state leakage current is presented in section 3. The implementation of the proposed circuit for measuring dark current is unveiled in section 4. Finally, a conclusion is made in the last section.

2. Test Socket Circuit for Measuring Dark Current

The detector in an IR FPA is a PN photovoltaic diode. Fig 1(b) shows its I-V characteristics with and without IR radiation. It is likable to know the dark current of the diode to quantify the detector's performance. In normal case, for an InSb IR diode, the dark current is in the range from several pA to a hundred pA under applying a small reverse bias. The smaller the dark current, the better performance the detector will be. And if the dark current is out of the range, then the detector will be useless. To measure the dark current, it can be directly measured by probing at the bump pad of the detectors. However, the direct probing method needs expensive equipment and time consuming operations. Besides, the uncertainty of the probing contact and interference from the open environment would make the measurement being more difficult.

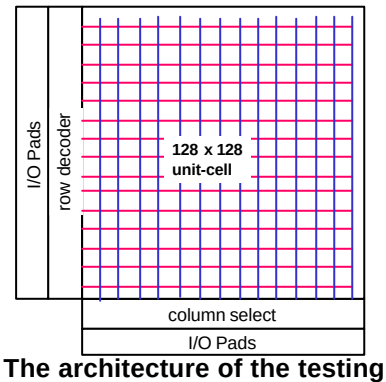


Fig 3 : The architecture of the testing circuit

To overcome the difficulties, a test socket circuit chip for measuring dark current is proposed [13]. This chip compounds with the detector array via flip-chip technology can inherently segregate and reduce the environment interference. The proposed circuit is shown in Fig 3. Its operation resembles the addressing of random access memory. Each detector in the FPA will be directly accessed through the address lines. When addressed, it will construct a measuring path connecting the selected detector to an I/O pad through a series of MOS switches operated at ON-state, as shown in Fig 4. A set of swept reverse bias steps is applied into the addressed detector through the constructed path to measure the I-V characteristics of dark currents.

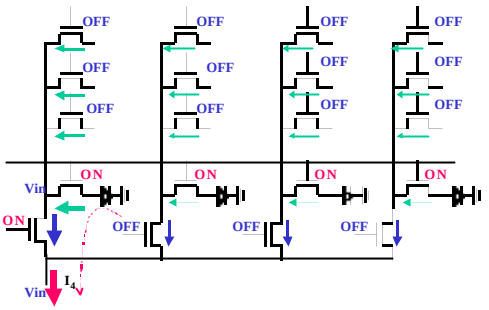


Fig 4 : The selection of a detector

Since the dark current is about from several pA to a hundred pA, the voltage drop along the measuring path due to the parasitic resistance and MOS's ON-resistance, R_{ON}, can be neglected. Nevertheless, there will be a lot of OFF-state MOSs tied to the measuring path, the number depends on the array size. All these OFF-state MOSs will contribute a small OFF-state leakage current, I_{OFF}, to the path, and totally will have a fairly influence on the measuring result. Hence, it is desirable to calibrate these unwanted leakage currents to derive the accurate value of the detector's dark current. A novel calibration scheme to cancel the leakage current of OFF-state MOSs is proposed and demonstrated in the next section.

3. The Calibration Scheme for the MOS OFF-state Leakage Current

Due to the leakage current of OFF-state MOSs tied to the constructed measuring path, the measured current will have a large error as the array size increases. To calibrate these unwanted leakage currents, by slightly modifying the address decoder, we propose a scheme for canceling the leakage currents.

Since the detectors are arranged in a two dimensional array. A row address and a column address are used to select a detector. We use two extra control I/O pins to disable the row and column address selection independently. That is, even the address has been experienced, the output of the selected decoder can be still disabled by the two extra pins. Hence, there will have four cases. The four cases are simultaneously shown in Fig 5. Case 1 is that both the addressed row and column are disabled. Then all the MOSs are OFF. Case 2 is that the addressed row is disabled while the addressed column is still enabled. Therefore, only the addressed column MOS

is ON and all other MOSs are OFF. Case 3 is that the addressed row is ON and the addressed column is OFF. Thus, all the MOSs at the addressed row are ON, while all other MOSs are OFF. Case 4 is the normal selection. Both the addressed row and column are not disabled. Hence, all the MOSs along the addressed row and the MOS of the addressed column are ON, and the other MOSs are OFF.

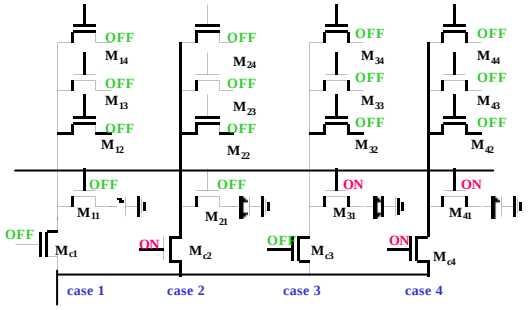


Fig. 5 : Four cases of the selection.

To examine the four cases, we will take a close look in the following paragraphs. (Without loss of generality, a 4 by 4 array is used.)

Case 1: Both the addressed row and column are disabled, as shown in Fig 6. All MOSs are OFF, the measured current, I_1, will be the sum of current flowing through the 4 columns of OFF-state MOSs. For each column, the current flowing through the column-MOS is the sum of the 4 I_{OFF} of the MOSs tied to this column. Hence, the current flowing at each OFF-state column-MOS is $I_{Mc1} = I_1/4$.

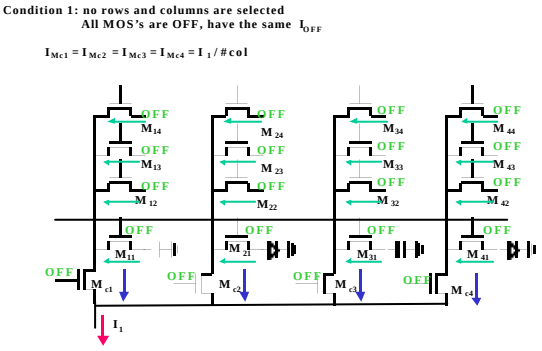


Fig. 6 : The case 1

Case 2: The addressed row is disabled, and the addressed column-MOS is ON. The other MOSs in the array are OFF except the addressed column-MOS, as shown in Fig 7. The measured current, I_2, is the sum of the current flowing through the addressed column-MOS and the other 3 OFF-state column-MOSs. The current flowing through the 3 OFF-state MOSs is the sum of 4 OFF-state MOSs tied to the respective column line. It is the same as case 1. While for the ON-state column, the applied reverse voltage appears at the column line, although the 4 MOSs tied to this addressed column are all OFF, they have different voltage bias from the case 1. The OFF-state MOSs will have a little larger leakage current than those of in case 1. Hence, the current flowing in the addressed column-MOS is equal to $I_2 - (I_1/4)*3$. And the current flowing in OFF-state MOSs tied to the selected column is equal to $[I_2-(I_1/4)*3]/4$.

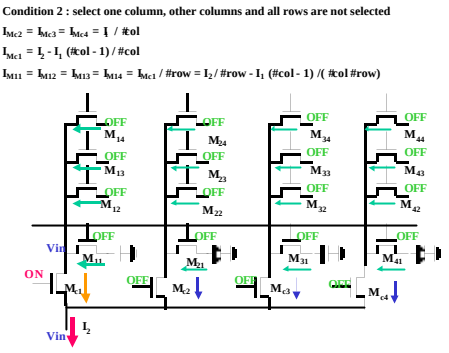


Fig. 7 : The case 2

Case 3: The addressed column is disabled while the addressed row is selected. All the column-MOSs are OFF, and the addressed row-MOSs are ON, as shown in Fig 8. The 4 MOSs of the selected row are ON and the others are OFF. The measured current, I_3, is the sum of 4 OFF-state column-MOSs. For each column-MOS, the current is the sum of 3 OFF-state MOSs and one ON-state MOS. (Notice that: since the row is selected, the dark current of the detector will flow through the ON-state MOS to charge the column line, and change the bias of the MOSs tied in the column. Hence the I_{OFF} is different from those of cases 1 and 2.) All 4 column-MOSs have the same bias, then the current flowing in column-MOS is equal to $I_3/4$.

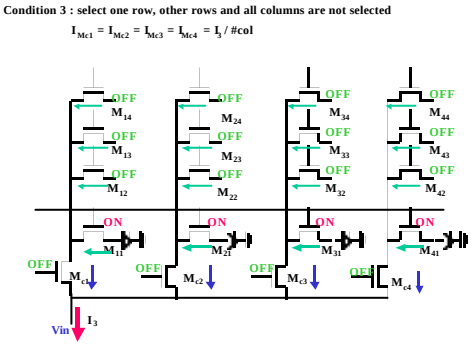


Fig. 8 : The case 3

Case 4: It is the normal selection. Both the addressed row and column are selected. The selected column-MOS and the row-MOSs are ON, and other MOSs are OFF, as shown in Fig 9. The measured current, I_4, is the sum of 3 OFF-state column-MOSs and one ON-state column-MOS. For the OFF-state column-MOSs, the current is the same as case 3. For the ON-state column-MOS, its curent is the sum of 3 OFF-state row-MOSs and one ON-state row-

MOS. For the OFF-state row-MOSs, the current is the same as case 2. For the ON-state row-MOS, its curent is the dark current of detector. Hence, the dark current $I_D = I_4 - 3(I_3/4) - 3[I_2 - (I_1/4)*3] / 4$.

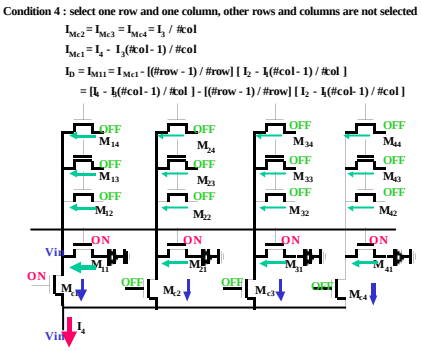
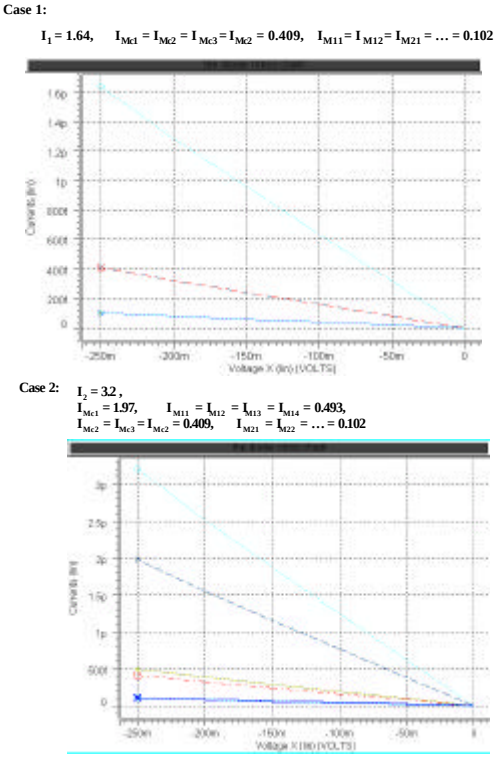


Fig 9 : The case 4

Based on the relationship of the 4 measured currents, we can derive the corrected detector dark current to be: $I_D = I_4 - k_1 I_3 - k_2 I_2 + k_1 k_2 I_1$, where k_1 = (#col–1)/#col, k_2= (#row–1)/#row, when #row and #col are large enough, (i.e., k_1, k_2 >>1), the dark current will be very close to $I_4 - I_3 - I_2 + I_1$.

Fig 10 is HSPICE simulation results of the 4 cases for a 4 x 4 array. The corresponding currents are listed at the top for each case.



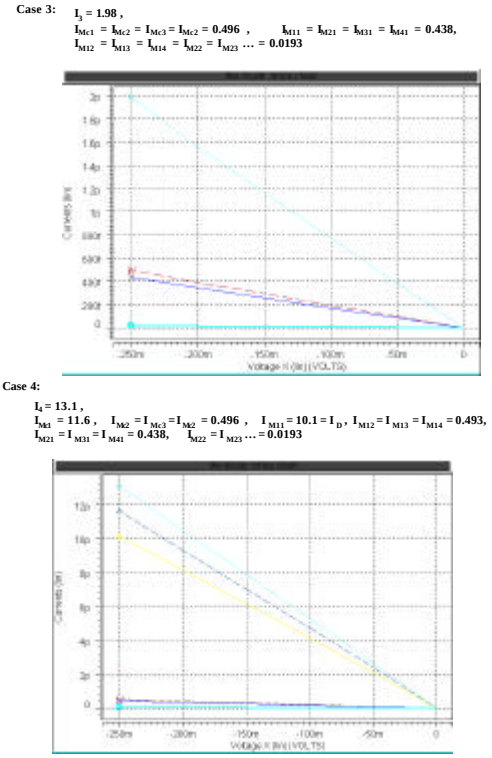


Fig 10 : Simulation of a 4x4 Array

4. Implementation

A test socket chip for 128 x 128 array has been designed and submitted to the MPC service of CIC (Chip Implementation Center). The unit cell is of the size 30um x 30um, including 3 NMOS switches, a small size P+_N-Well diode for testing purpose, and a bump pad. Fig 11 and 12 are the schematic and layout of the unit cell.

To verify the circuit before bump, a control signal, *test*, is used to select the testing-purpose diode in the unit cell. A forward bias voltage is then applied on the diode to verify the address decoder's function. After bump, the path is switched to bump pad where the IR detector attached, then the accurate dark currents are measured according to the calibration scheme described in section 3.

The layout for 128 x 128 IR FPA test socket circuit chip is shown in Fig 13. The technology used is UMC 0.5um 2P2M CMOS process. The chip size is 4518 um x 4364 um. The chip has been fabricated and is now under testing. Our next step is to combine this test socket scheme within a general readout circuit.

5. Conclusion

A test socket circuit chip for measuring dark currents of IR detector in a FPA is presented in this paper. The

chip employed a proposed calibration scheme to remedy the leakage current of OFF-state MOSs. Hence, a more accurate I-V characteristic of detectors can be derived. The resultant characteristics of the whole array can be used to construct a failure map and predict the gross yield.

The circuit chip had been submitted to CIC for fabrication using UMC 0.5um 2P2M process. The fabricated and verified testing chip will be interfaced with a PC to establish an automatic measuring system which is now under developing at Department of Electrical Engineering, National Chi Nan University.

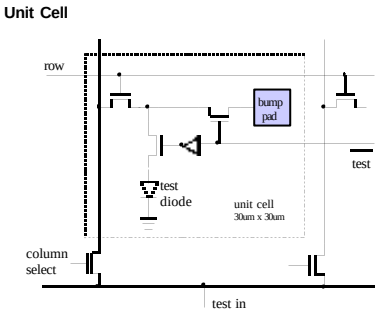


Fig 11 : The schematic of a unit cell

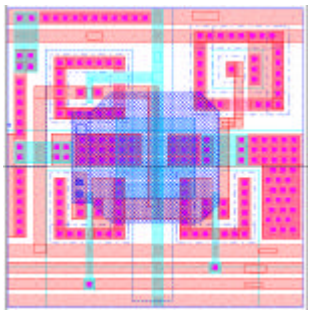


Fig 12 : The layout of a unit cell

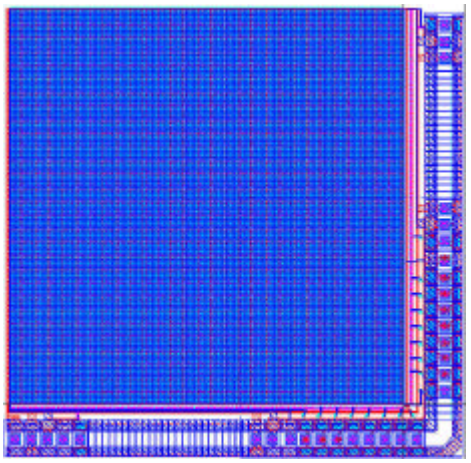


Fig 13 : The circuit for dark current measurement in 128 x 128 IR FPA

This work is sponsored by National Science Council Taiwan R.O.C., under contract number: NSC-89-2623-7-260-001. The authors would also thank the Chip Implementation Center (CIC) for their supports on chip fabrication.

6. References

[1] F. J. Crawford, "Electro-Optical Sensors Overview," IEEE Aerospace and Electronics Systems Magazines, Oct. 1998, pp.17-24.

[2] N. Itoh, K. Yanagisawa, T. Ichikawa, K. Tarusawa, and H. Kataza, "Kiso observatory near-infrared camera with a large format array," *in Proceedings of the SPIE, infrared technology XXI*, vol. 2552, pp. 430-437, 1995.

[3] D. A. Scribner, M. R. Kruer, and J. M. Killiany," Infrared focal-plane array technology," in *Proc. IEEE*, vol. 79, no.1, pp. 66-85, 1991

[4] E. R. Fossum and B. Pain," Infrared readout electronics for space science sensors: state of the art and future directions," *in Infrared Technology XIX*, Proc. SPIE 2020, pp. 262-285, 1993.

[5] Partrick J. Terado, Ira W. Levin, and E. Neil Lewis, "Indium antimonide(lnSb) Focal Plane Array (FPA) Detection for Near-Infrared Imaging Microscopy", Applied, Spcctroscopy Vol. 48(5), pp.607-615(1994)

[6] Ilan Bloom and Yael Nemirovsky," Quantum Efficiency and Crosstalk of an Improved Backside-Illuminated Indium Antimonide Focal-plane Array", IEEE Transactions on Electron Devices. Vol.38, No.8, pp.1792-1796 (1991).

[7] Ilan Bloom and Yael Nemirovsky, "Bulk Lifetime Determination of Etch-Thinned InSb Wafers for Two-Dimensional Infrared Focal Plane Array", IEEE Transactions on Electron Devices, Vol.39, NO.4, pp.809-812 (1992).

[8] C. C. Hsieh, C. Y. Wu, F. W. Jih and T. P. Sun , "Focal Plane Arrays and CMOS Readout Techniques of Infrared Imaging Systems," IEEE Trans. on Circuits and Systems for Video Technology, Aug. 1997.

[9] C. Y. Wu, C. C. Hsieh, "New Design Techniques for a CMOS Current Readout Integration Circuits for Infrared Detector Arrays," Opt. Engineering, Jan. 1995.

[10] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun and Horng Chang , "A New CMOS Readout Circuit Design for the IR FPA with Adaptive Gain Control and Current Mode Background Suppression" IEEE Proc. ISCAS'96, 1996.

[11] C. C. Hsieh, C. Y. Wu and T. P. Sun, "A New Cryogenic CMOS Readout Structure for Infrared Focal Plane Array," IEEE Journal of Solid-State Circuits, Aug. 1997, pp1192-1199.

[12] C. C. Hsieh, C. Y. Wu, T. P. Sun, F. W. Jih and Y. T. Cherng, "High Performance CMOS Buffered gate Modulation Input (BGMI) Readout Circuits for IR FPA," IEEE Journal of Solid-State Circuits, Aug. 1998, pp1188-1198.

[13] M. L. Sheu, T. P. Sun and M. C. Shie, "Measurement of Dark Current of Infrared Detector in Focal Plane Array," Proceeding of 12th VLSI Design/CAD Workshop, Aug. 2001, B3-8.